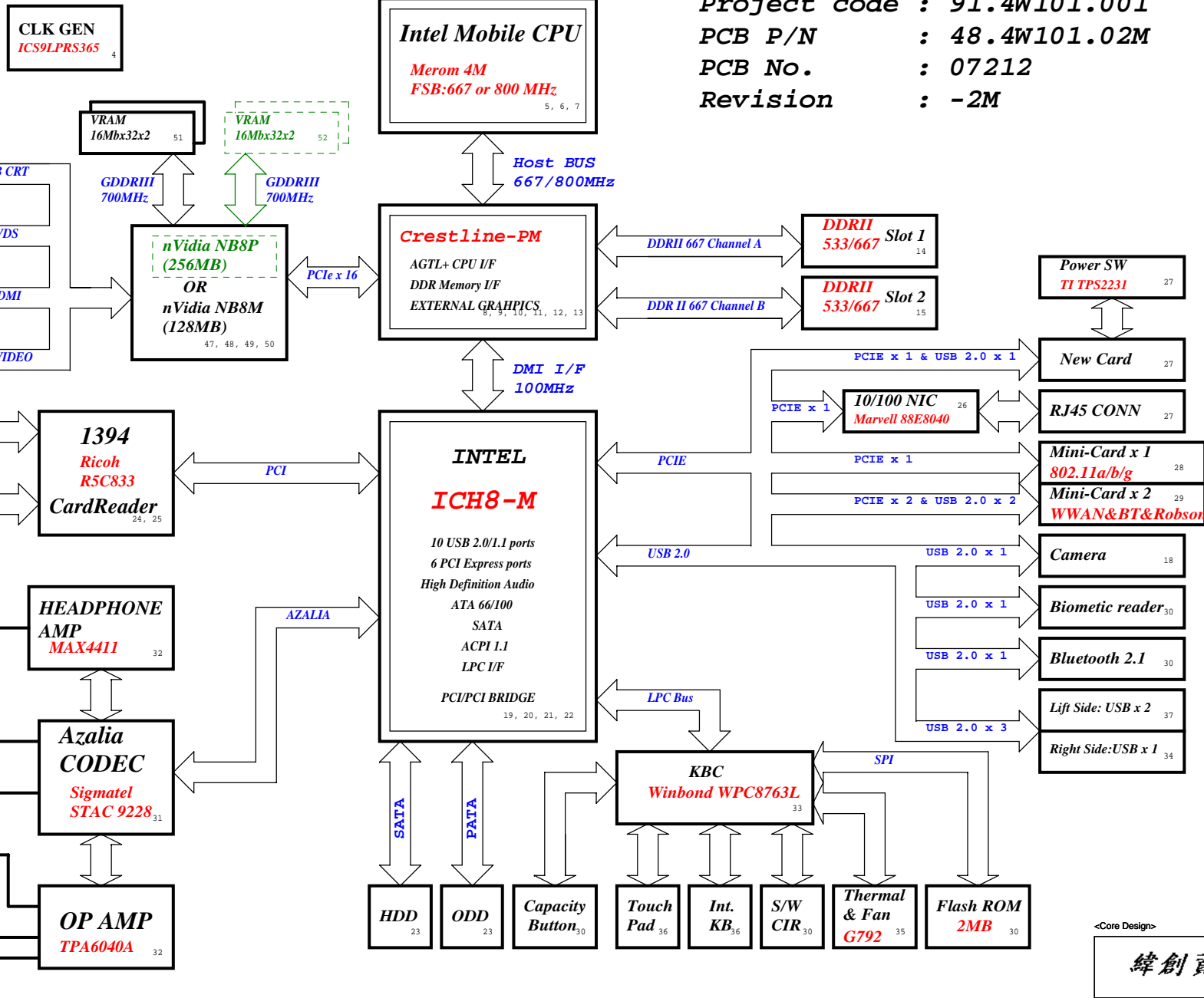


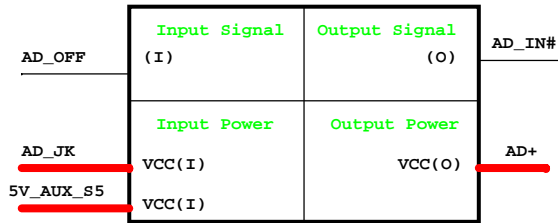
Hawke Intel Discrete Block Diagram



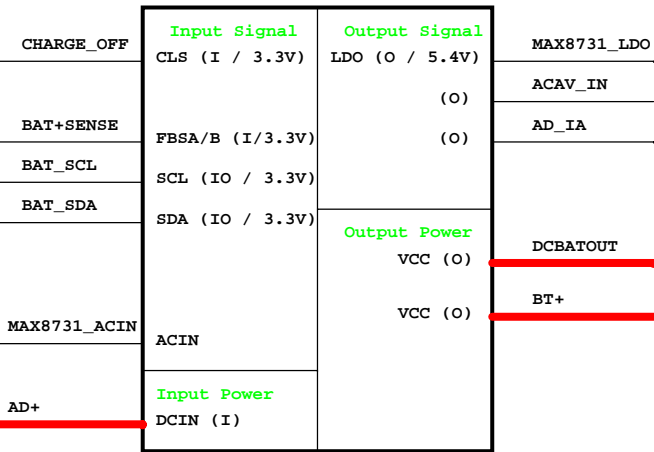
Project code : 91.4W101.001
PCB P/N : 48.4W101.02M
PCB No. : 07212
Revision : -2M

BATTERY CHARGER MAX8731A		38
INPUTS	OUTPUTS	
AD+ BAT+	DCBATOUT	
SYSTEM DC/DC TPS51120		39
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	
SYSTEM DC/DC TPS5117		42, 43
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0 1D8V_S3	
SYSTEM DC/DC TPS51100		44
INPUTS	OUTPUTS	
1D8V_S3	0D9V_S3	
SYSTEM DC/DC RT9018		44
INPUTS	OUTPUTS	
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0	
VGA DC/DC TPS5117		53
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFX_CORE_S0	
CPU DC/DC ISL6262A		40
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
PCB LAYER		
L1:TOP		
L2:GND		
L3:Signal		
L4:Signal		
L5:VCC		
L6:Singal		
L7:GND		
L8:BOT		

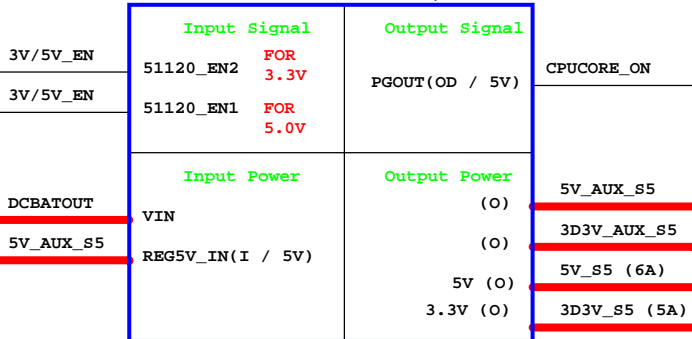
Adapter



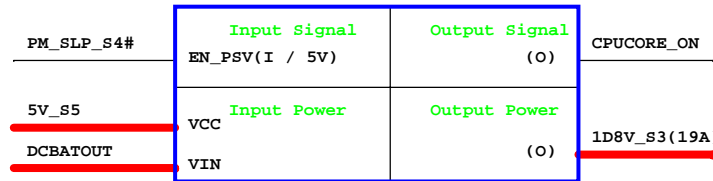
Charger MAX8731A



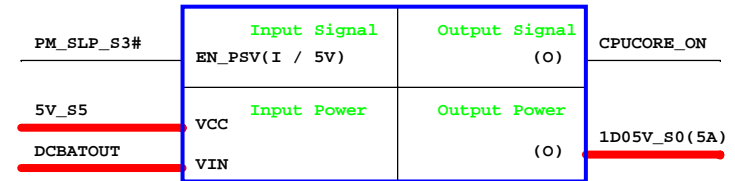
TI TPS51120 3D3V/5V



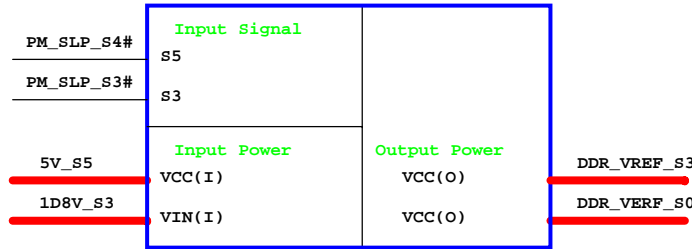
TPS51117 1D8V



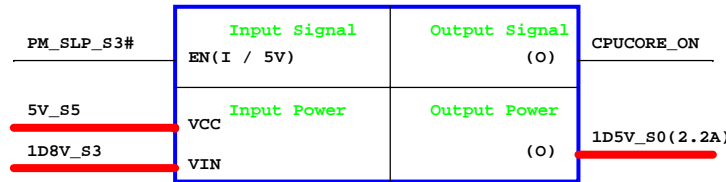
TPS51117 1D05V



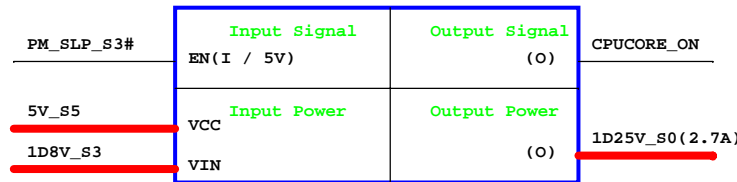
TI TPS51100 0.9V/DDR_VREF_S3



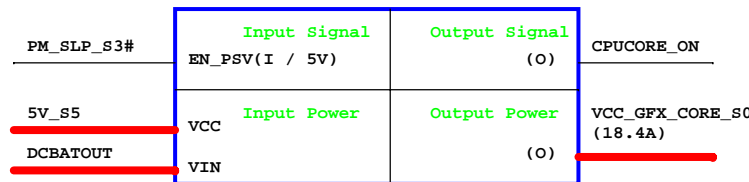
RT9018A 1D5V



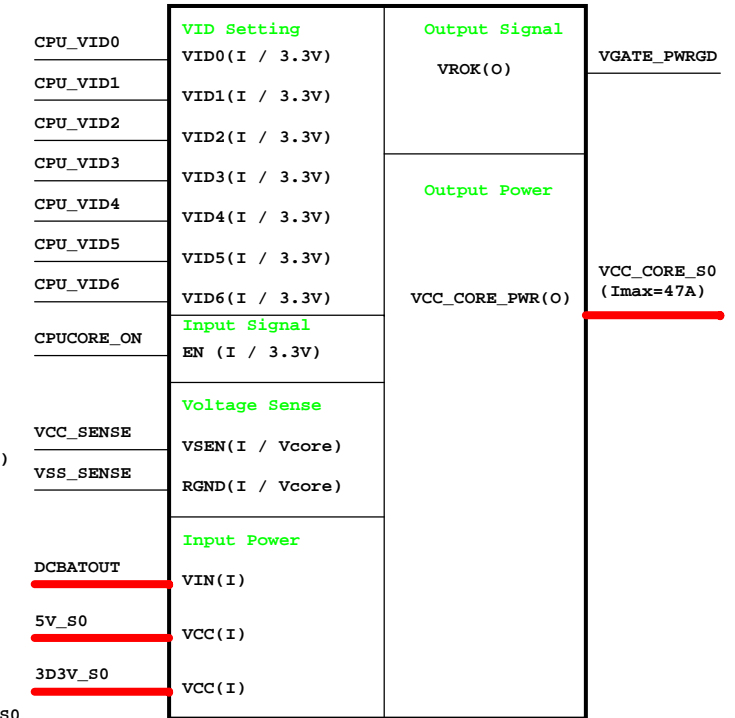
RT9018A 1D25V



TPS51117 VGA_CORE



ISL6262A CPU_CORE



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Block Diagram		
Size A3	Document Number Hawke-Intel	Rev -2
Date: Thursday, November 22, 2007	Sheet 2 of 58	

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP_Tp3	AZ_DOUT_ICH	Description	
0	0	RSVD	
0	1	Enter XOR Chain	
1	0	Normal Operation(default)	
1	1	Set PCIE port config bit1	

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

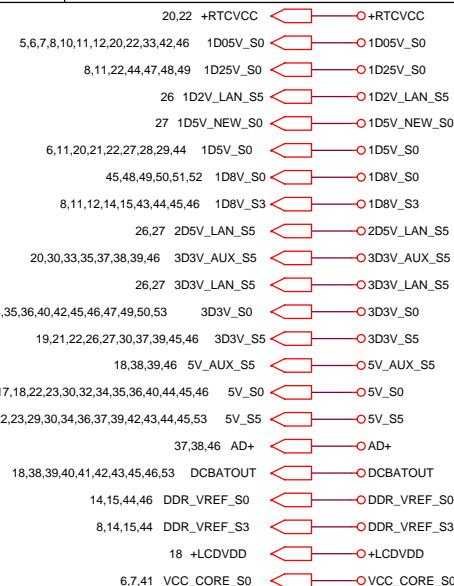
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CI_RST#	TBD



PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A C	0	0

USB TABLE

USB0	Ext Lift Side (Bottom)
USB1	Ext Lift Side (Top)
USB2	Ext Right Side
USB3	N/A
USB4	WWAN
USB5	Bluetooth
USB6	Camera
USB7	Biometric
USB8	Express Card
USB9	3rd mini card

PCIE Routing

LANE1	10/100M Bit LOM
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN
LANE4	BT/UWB/Robson
LANE5	Express Card
LANE6	N/A

<Core Design>

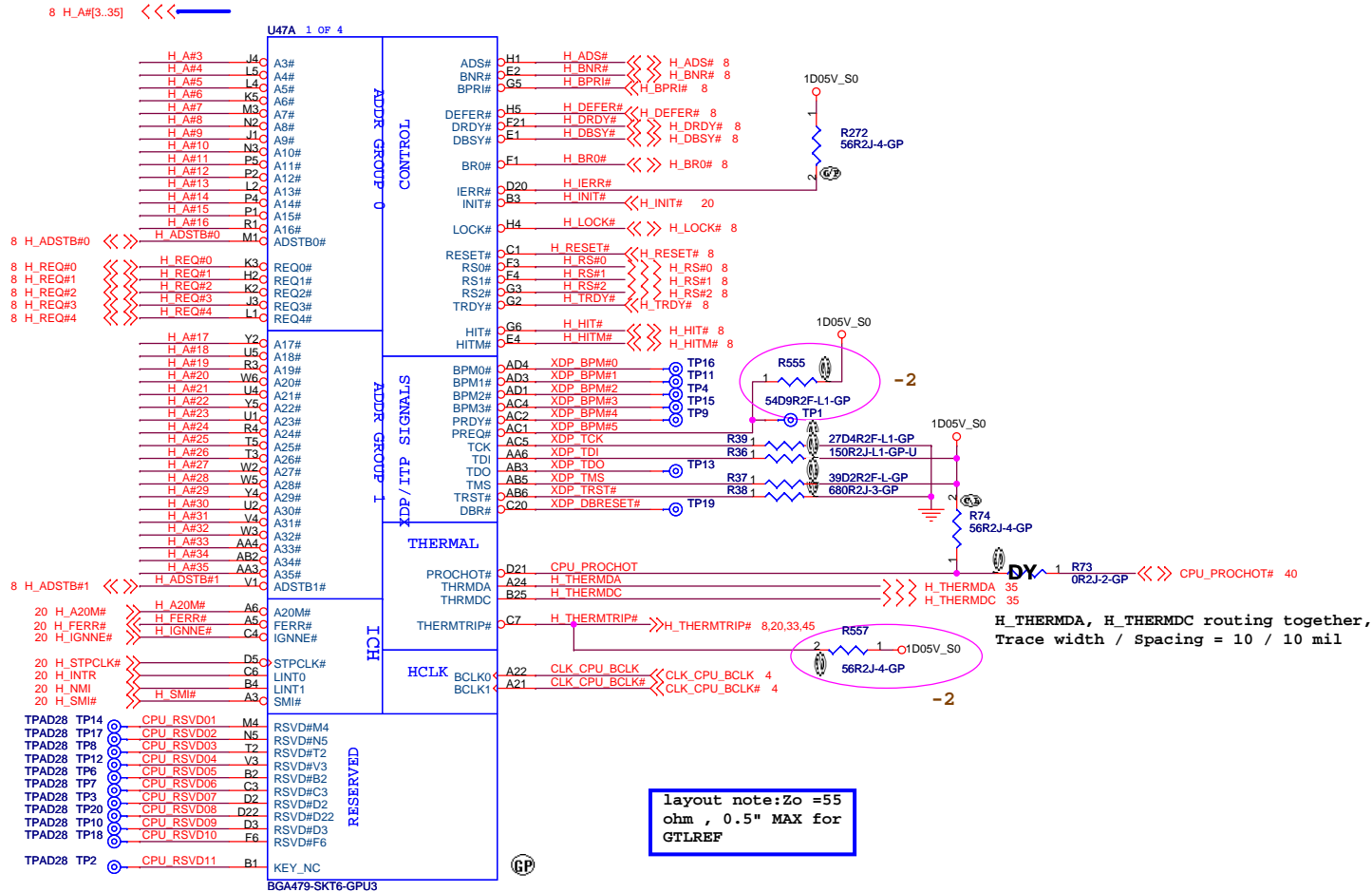
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Table of Content	
Size A3	Document Number	Hawke-Intel		Rev -2
Date: Thursday, November 22, 2007	Sheet 3	of		58

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes★ number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation



Main source : 62.10079.021 Tyco 2-1871873-4
2nd source : 62.10040.221 Foxconn PZ47827-274M-41

<Core Design>

8 H_D# [0.63] <<>>

8 H_DSTBN#0
8 H_DSTBP#0
8 H_DINV#0

8 H_DSTBN#1
8 H_DSTBP#1
8 H_DINV#1

4.8 CPU_BSEL0
4.8 CPU_BSEL1
4.8 CPU_BSEL2

PLACE C617 close to the TEST4 PIN,
make sure TEST3,TEST4,TEST5 trace
routing is reference to GND and
away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

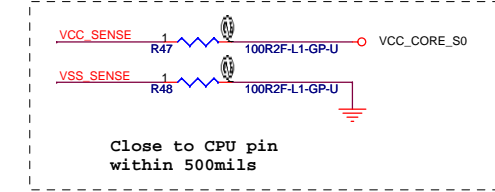
Resistor Placed
within 0.5" of CPU
pin. Trace should
be at least 25 mils
away from any other
toggling signal .
COMP[0,2] trace
width is 18 mils.
COMP[1,3] trace
width is 4 mils .

VCC_CORE_S0

VCC_CORE_S0

layout note:
place C618 near
PIN B26

Length match within
25 mils . The trace
width/space/other is
20/7/25 .

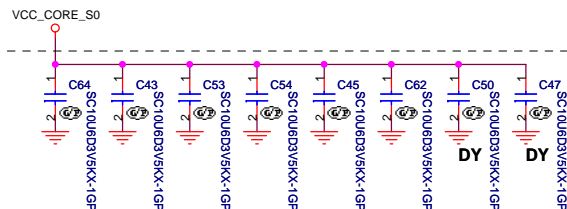


U47D 4 OF 4

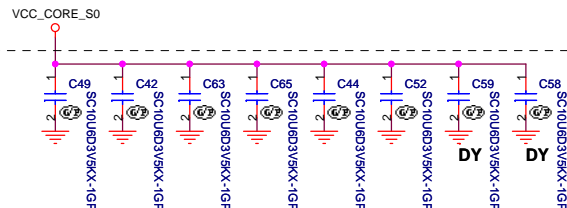
A4	VSS	VSS	P6
A8	VSS	VSS	P21
A11	VSS	VSS	P24
A14	VSS	VSS	R2
A16	VSS	VSS	R5
A19	VSS	VSS	R22
A23	VSS	VSS	R25
AF2	VSS	VSS	T1
B6	VSS	VSS	T4
B8	VSS	VSS	T23
B11	VSS	VSS	T26
B13	VSS	VSS	U3
B16	VSS	VSS	U6
B19	VSS	VSS	U21
B21	VSS	VSS	U24
B24	VSS	VSS	V2
C5	VSS	VSS	V5
C8	VSS	VSS	V22
C11	VSS	VSS	V25
C14	VSS	VSS	W1
C16	VSS	VSS	W4
C19	VSS	VSS	W23
C2	VSS	VSS	W26
C22	VSS	VSS	Y3
C25	VSS	VSS	Y6
D1	VSS	VSS	Y21
D4	VSS	VSS	Y24
D8	VSS	VSS	AA2
D11	VSS	VSS	AA5
D13	VSS	VSS	AA8
D16	VSS	VSS	AA11
D19	VSS	VSS	AA14
D23	VSS	VSS	AA16
D26	VSS	VSS	AA19
E3	VSS	VSS	AA22
E6	VSS	VSS	AA25
E8	VSS	VSS	AB1
E11	VSS	VSS	AB4
E14	VSS	VSS	AB8
E16	VSS	VSS	AB11
E19	VSS	VSS	AB13
E21	VSS	VSS	AB16
E24	VSS	VSS	AB19
F5	VSS	VSS	AB23
F8	VSS	VSS	AB26
F11	VSS	VSS	AC3
F13	VSS	VSS	AC6
F16	VSS	VSS	AC8
F19	VSS	VSS	AC11
F2	VSS	VSS	AC14
F22	VSS	VSS	AC16
F25	VSS	VSS	AC19
G4	VSS	VSS	AC21
G1	VSS	VSS	AC24
G23	VSS	VSS	AD2
G26	VSS	VSS	AD5
H3	VSS	VSS	AD8
H6	VSS	VSS	AD11
H21	VSS	VSS	AD13
H24	VSS	VSS	AD16
J2	VSS	VSS	AD19
J5	VSS	VSS	AD22
J22	VSS	VSS	AD25
J25	VSS	VSS	AE1
K1	VSS	VSS	AE4
K4	VSS	VSS	AE8
K23	VSS	VSS	AE11
K26	VSS	VSS	AE14
L3	VSS	VSS	AE16
L6	VSS	VSS	AE19
L21	VSS	VSS	AE23
L24	VSS	VSS	AE26
M2	VSS	VSS	A2
M5	VSS	VSS	AF6
M22	VSS	VSS	AF8
M25	VSS	VSS	AF11
N1	VSS	VSS	AF13
N4	VSS	VSS	AF16
N23	VSS	VSS	AF19
N26	VSS	VSS	AF21
P3	VSS	VSS	A25
	VSS	VSS	AF25

BGA479-SKT6-GPU3

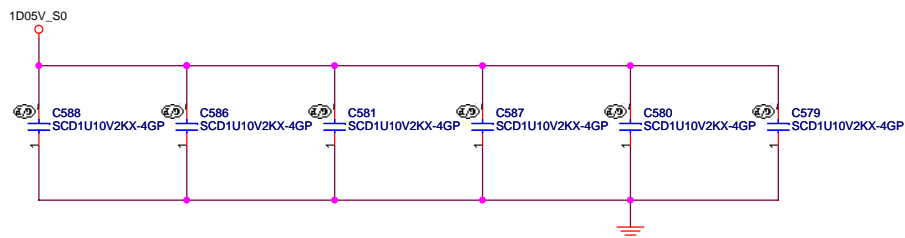
Place these capacitors on L1
(North side ,Secondary Layer)



Place these capacitors on L1
(North side ,Secondary Layer)



Mid Frequencd
Decoupling

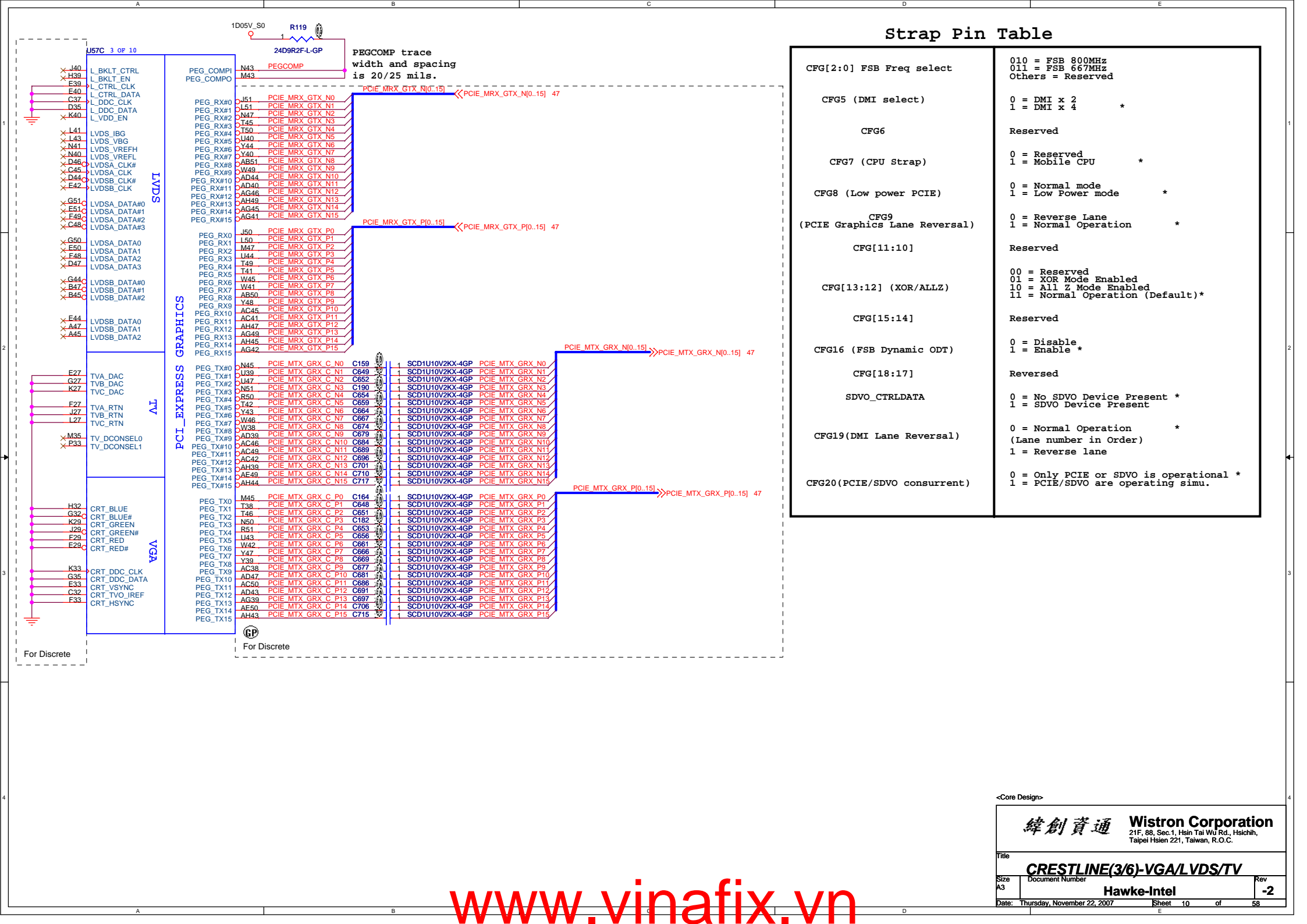


Place these
inside socket
cavity on L1
(North side
Secondary)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		Meron(3/3)-GND&Bypass	
Size	Document Number	Rev	
A3	Hawke-Intel	-2	
Date:	Thursday, November 22, 2007	Sheet	7 of 58



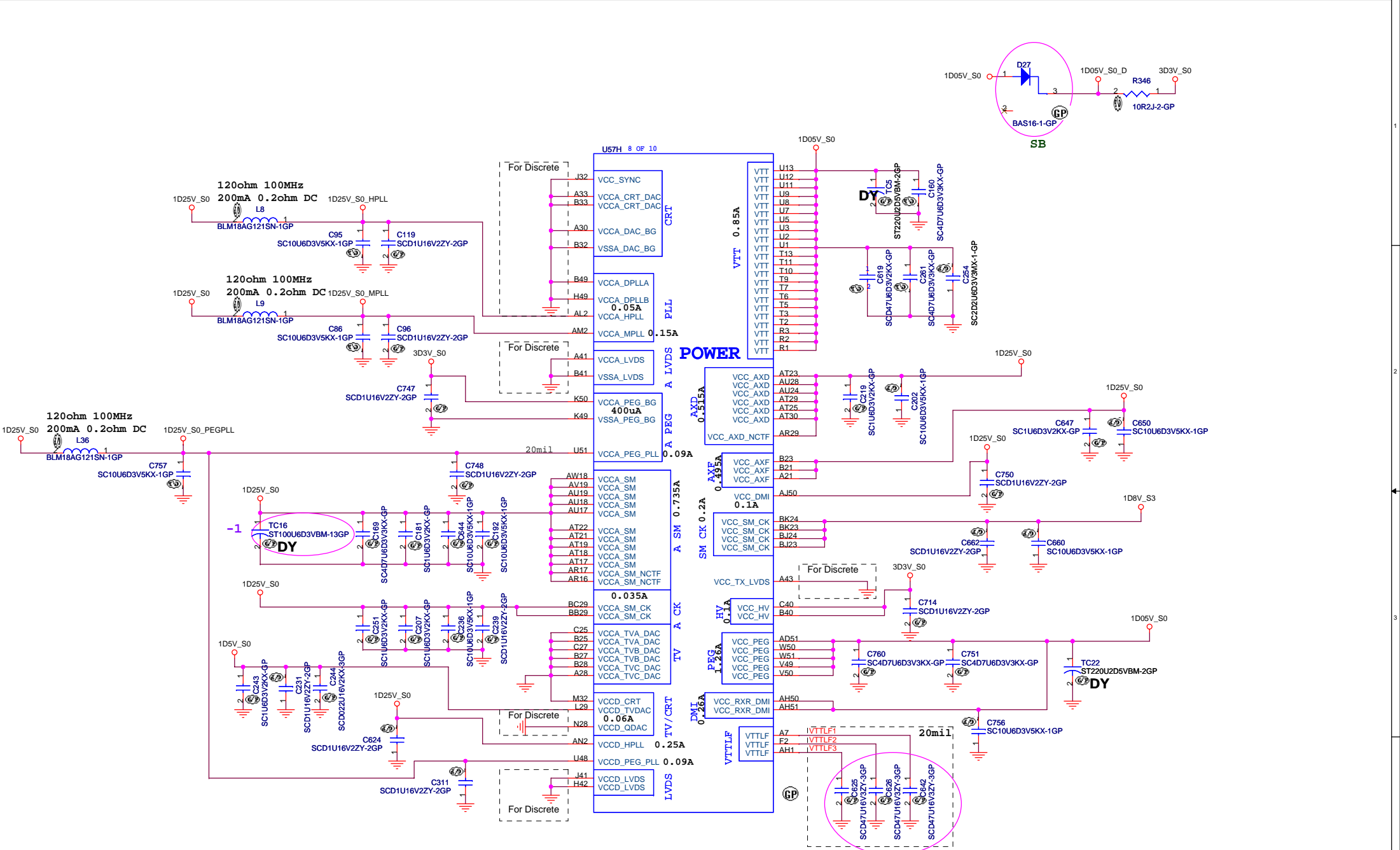
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse lane *
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CRESTLINE(3/6)-VGA/LVDS/TV	
Size	Document Number	Hawke-Intel	Rev
A3			-2
Date:	Thursday, November 22, 2007	Sheet	10 of 58





U57I 9 OF 10

A13	VSS	VSS	AW24
A15	VSS	VSS	AW29
A17	VSS	VSS	AW32
A24	VSS	VSS	AW5
AA21	VSS	VSS	AW7
AA24	VSS	VSS	AY10
AA29	VSS	VSS	AY24
AB20	VSS	VSS	AY37
AB23	VSS	VSS	AY42
AB26	VSS	VSS	AY43
AB28	VSS	VSS	AY45
AB31	VSS	VSS	AY47
AC10	VSS	VSS	AY50
AC13	VSS	VSS	B10
AC3	VSS	VSS	B20
AC39	VSS	VSS	B24
AC43	VSS	VSS	B29
AD1	VSS	VSS	B30
AD21	VSS	VSS	B35
AD26	VSS	VSS	B38
AD29	VSS	VSS	B43
AD3	VSS	VSS	B46
AD41	VSS	VSS	B5
AD45	VSS	VSS	B8
AD49	VSS	VSS	BA1
AD5	VSS	VSS	BA17
AD50	VSS	VSS	BA18
AD8	VSS	VSS	BA2
AE10	VSS	VSS	BA24
AE14	VSS	VSS	BB12
AE6	VSS	VSS	BB25
AF20	VSS	VSS	BB40
AF23	VSS	VSS	BB44
AF24	VSS	VSS	BB49
AF31	VSS	VSS	BB8
AG2	VSS	VSS	BC16
AG38	VSS	VSS	BC24
AG43	VSS	VSS	BC25
AG47	VSS	VSS	BC36
AG50	VSS	VSS	BC40
AH3	VSS	VSS	BC51
AH40	VSS	VSS	BD13
AH41	VSS	VSS	BD2
AH7	VSS	VSS	BD28
AH9	VSS	VSS	BD45
AJ11	VSS	VSS	BD48
AJ13	VSS	VSS	BD5
AJ21	VSS	VSS	BE1
AJ24	VSS	VSS	BE19
AJ29	VSS	VSS	BE23
AJ32	VSS	VSS	BE30
AJ43	VSS	VSS	BE42
AJ45	VSS	VSS	BE51
AJ49	VSS	VSS	BE8
AK20	VSS	VSS	BF12
AK21	VSS	VSS	BF16
AK26	VSS	VSS	BF36
AK28	VSS	VSS	BG19
AK31	VSS	VSS	BG2
AK51	VSS	VSS	BG24
AL1	VSS	VSS	BG29
AM11	VSS	VSS	BG39
AM13	VSS	VSS	BG48
AM3	VSS	VSS	BG5
AM4	VSS	VSS	BG51
AM41	VSS	VSS	BH17
AM45	VSS	VSS	BH30
AN1	VSS	VSS	BH44
AN38	VSS	VSS	BH46
AN39	VSS	VSS	BH8
AN43	VSS	VSS	BJ11
AN5	VSS	VSS	BJ13
AN7	VSS	VSS	BJ38
AP4	VSS	VSS	BJ4
AP48	VSS	VSS	BJ42
AP50	VSS	VSS	BJ46
AR11	VSS	VSS	BK12
AR2	VSS	VSS	BK17
AR39	VSS	VSS	BK25
AR44	VSS	VSS	BK29
AR47	VSS	VSS	BK36
AT10	VSS	VSS	BK40
AT14	VSS	VSS	BK44
AT41	VSS	VSS	BK6
AT49	VSS	VSS	BK8
AU1	VSS	VSS	BL11
AU23	VSS	VSS	BL13
AU29	VSS	VSS	BL19
AU3	VSS	VSS	BL22
AU36	VSS	VSS	BL37
AU49	VSS	VSS	BL47
AU51	VSS	VSS	C12
AV39	VSS	VSS	C16
AV48	VSS	VSS	C19
AW1	VSS	VSS	C28
AW12	VSS	VSS	C29
AW16	VSS	VSS	C33
		VSS	C36
		VSS	C41

VSS

U57J10 OF 10

C46	VSS	VSS	W11
C50	VSS	VSS	W39
C7	VSS	VSS	W43
D13	VSS	VSS	W47
D24	VSS	VSS	W5
D3	VSS	VSS	W7
D32	VSS	VSS	Y13
D39	VSS	VSS	Y2
D45	VSS	VSS	Y41
D49	VSS	VSS	Y45
E10	VSS	VSS	Y49
E16	VSS	VSS	Y5
E24	VSS	VSS	Y50
E28	VSS	VSS	Y11
E32	VSS	VSS	P29
E47	VSS	VSS	T29
F19	VSS	VSS	T31
F36	VSS	VSS	T33
F4	VSS	VSS	R28
F40	VSS		
F50	VSS		
G1	VSS		
G13	VSS		
G16	VSS	VSS	AA32
G19	VSS	VSS	AB32
G24	VSS	VSS	AD32
G28	VSS	VSS	AF28
G29	VSS	VSS	AF29
G33	VSS	VSS	AT27
G42	VSS	VSS	AV25
G45	VSS	VSS	HS0
G48	VSS		
G8	VSS		
H24	VSS		
H28	VSS		
H4	VSS		
H45	VSS		
J11	VSS		
J16	VSS		
J2	VSS		
J24	VSS		
J28	VSS		
J33	VSS		
J35	VSS		
J39	VSS		
K12	VSS		
K47	VSS		
K8	VSS		
L1	VSS		
L17	VSS		
L20	VSS		
L24	VSS		
L28	VSS		
L3	VSS		
L33	VSS		
L49	VSS		
M28	VSS		
M42	VSS		
M46	VSS		
M49	VSS		
M5	VSS		
M50	VSS		
M9	VSS		
N11	VSS		
N14	VSS		
N17	VSS		
N29	VSS		
N32	VSS		
N36	VSS		
N39	VSS		
N44	VSS		
N49	VSS		
N7	VSS		
P19	VSS		
P2	VSS		
P23	VSS		
P3	VSS		
P50	VSS		
R49	VSS		
T39	VSS		
T43	VSS		
T47	VSS		
U41	VSS		
U45	VSS		
U50	VSS		
V2	VSS		
V3	VSS		

VSS

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRESTLINE(6/6)-PWR/GND

Size

Document Number

Hawke-Intel

Rev

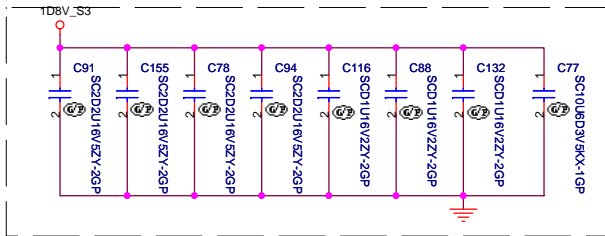
-2

Date: Thursday, November 22, 2007

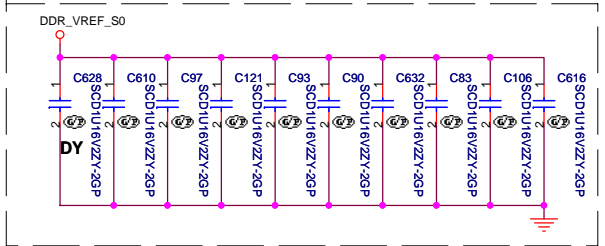
Sheet 13 of 58

www.vinafix.vn

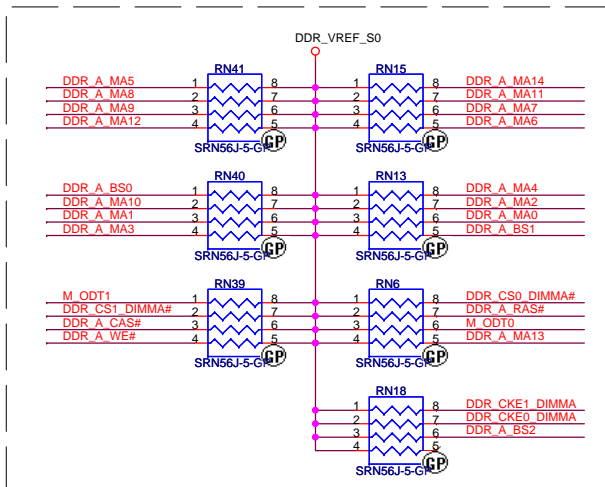
Layout Note:
Place near DM1



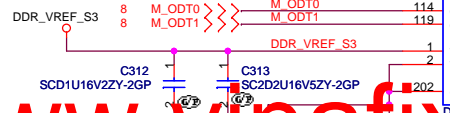
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



change to 8P4R

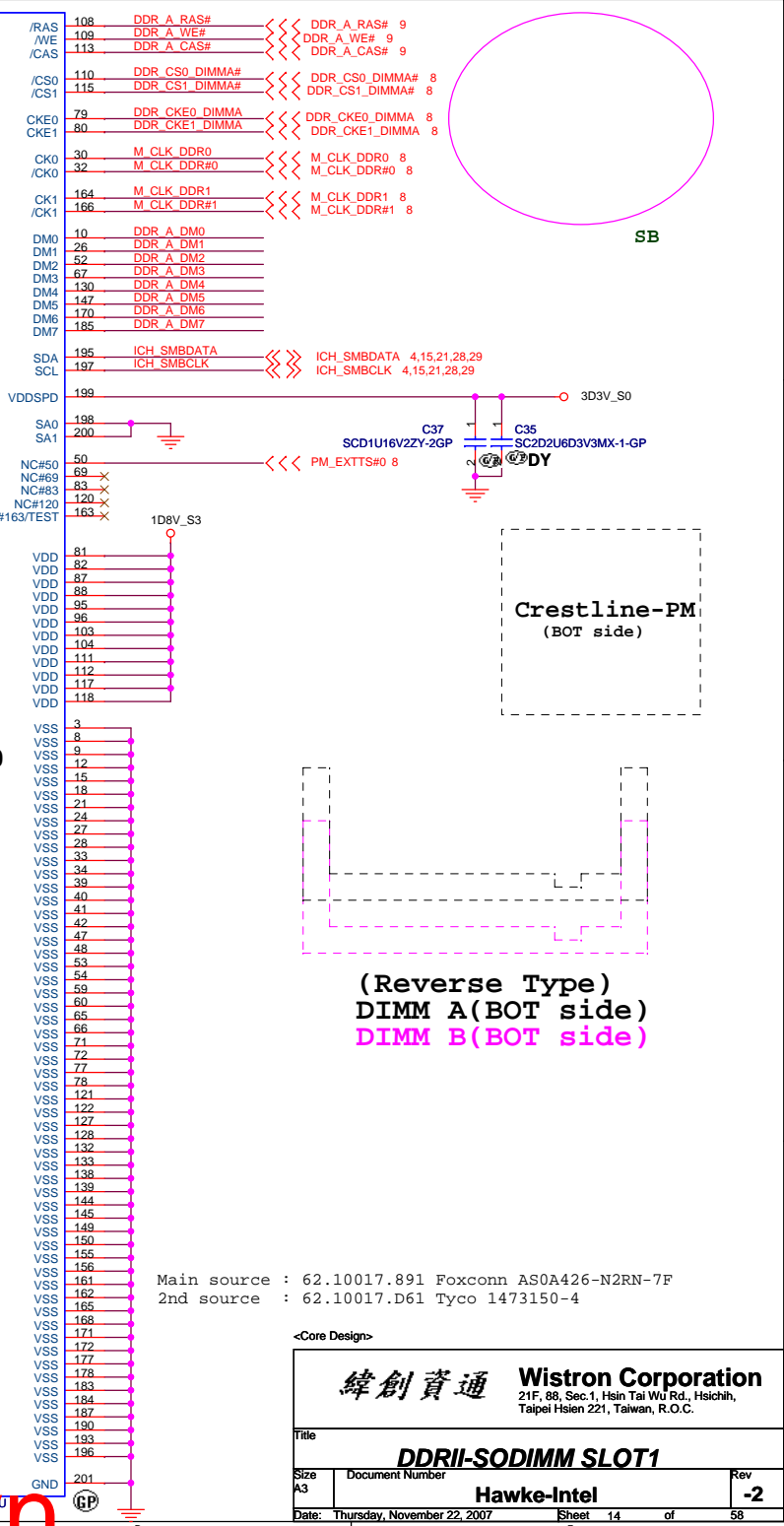


Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"



DDR_A_MA0	102	A0	/RAS	108	DDR_A_RAS#	<<<>>>	DDR_A_RAS# 9
DDR_A_MA1	101	A1	/WE	109	DDR_A_WE#	<<<>>>	DDR_A_WE# 9
DDR_A_MA2	100	A2	/CAS	113	DDR_A_CAS#	<<<>>>	DDR_A_CAS# 9
DDR_A_MA3	99	A3					
DDR_A_MA4	98	A4					
DDR_A_MA5	97	A5					
DDR_A_MA6	96	A6					
DDR_A_MA7	95	A7					
DDR_A_MA8	94	A8					
DDR_A_MA9	93	A9					
DDR_A_MA10	92	A10/AP					
DDR_A_MA11	91	A11					
DDR_A_MA12	90	A12					
DDR_A_MA13	89	A13					
DDR_A_MA14	88	A14					
DDR_A_MA15	87	A15					
DDR_A_MA16	86	A16/BA2					
DDR_A_MA17	85						
DDR_A_MA18	84						
DDR_A_MA19	83						
DDR_A_MA20	82						
DDR_A_MA21	81						
DDR_A_MA22	80						
DDR_A_MA23	79						
DDR_A_MA24	78						
DDR_A_MA25	77						
DDR_A_MA26	76						
DDR_A_MA27	75						
DDR_A_MA28	74						
DDR_A_MA29	73						
DDR_A_MA30	72						
DDR_A_MA31	71						
DDR_A_MA32	70						
DDR_A_MA33	69						
DDR_A_MA34	68						
DDR_A_MA35	67						
DDR_A_MA36	66						
DDR_A_MA37	65						
DDR_A_MA38	64						
DDR_A_MA39	63						
DDR_A_MA40	62						
DDR_A_MA41	61						
DDR_A_MA42	60						
DDR_A_MA43	59						
DDR_A_MA44	58						
DDR_A_MA45	57						
DDR_A_MA46	56						
DDR_A_MA47	55						
DDR_A_MA48	54						
DDR_A_MA49	53						
DDR_A_MA50	52						
DDR_A_MA51	51						
DDR_A_MA52	50						
DDR_A_MA53	49						
DDR_A_MA54	48						
DDR_A_MA55	47						
DDR_A_MA56	46						
DDR_A_MA57	45						
DDR_A_MA58	44						
DDR_A_MA59	43						
DDR_A_MA60	42						
DDR_A_MA61	41						
DDR_A_MA62	40						
DDR_A_MA63	39						
DDR_A_MA64	38						
DDR_A_MA65	37						
DDR_A_MA66	36						
DDR_A_MA67	35						
DDR_A_MA68	34						
DDR_A_MA69	33						
DDR_A_MA70	32						
DDR_A_MA71	31						
DDR_A_MA72	30						
DDR_A_MA73	29						
DDR_A_MA74	28						
DDR_A_MA75	27						
DDR_A_MA76	26						
DDR_A_MA77	25						
DDR_A_MA78	24						
DDR_A_MA79	23						
DDR_A_MA80	22						
DDR_A_MA81	21						
DDR_A_MA82	20						
DDR_A_MA83	19						
DDR_A_MA84	18						
DDR_A_MA85	17						
DDR_A_MA86	16						
DDR_A_MA87	15						
DDR_A_MA88	14						
DDR_A_MA89	13						
DDR_A_MA90	12						
DDR_A_MA91	11						
DDR_A_MA92	10						
DDR_A_MA93	9						
DDR_A_MA94	8						
DDR_A_MA95	7						
DDR_A_MA96	6						
DDR_A_MA97	5						
DDR_A_MA98	4						
DDR_A_MA99	3						
DDR_A_MA100	2						
DDR_A_MA101	1						

REVERSE TYPE High 5.2 mm



(Reverse Type)
DIMM A(BOT side)
DIMM B(BOT side)

Main source : 62.10017.891 Foxconn AS0A426-N2RN-7F
2nd source : 62.10017.D61 Tyco 1473150-4

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDRII-SODIMM SLOT1

Size A3

Document Number

Hawke-Intel

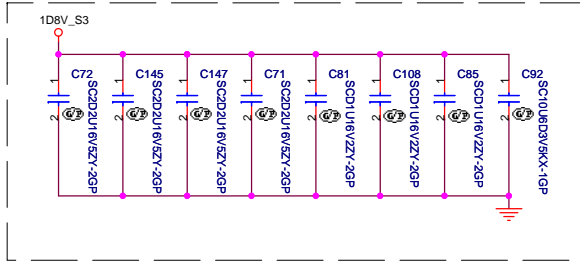
Date: Thursday, November 22, 2007

Sheet 14 of 58

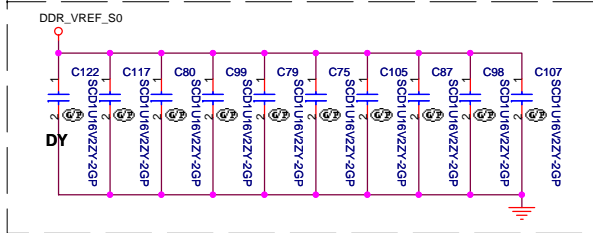
Rev

-2

Layout Note:
Place near DM2

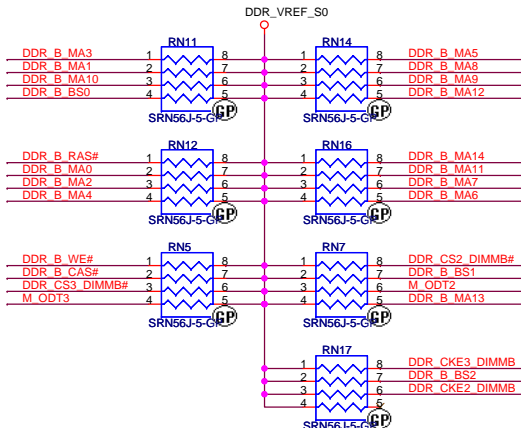


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



9 DDR_B_DQS#[0..7] <<>>>>
9 DDR_B_D[0..63] <<>>>>
9 DDR_B_DM[0..7] >>>>
9 DDR_B_DQS#[0..7] <<>>>>
9 DDR_B_MA[0..14] >>>>
9 DDR_B_BS[0..2] >>>>

Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"



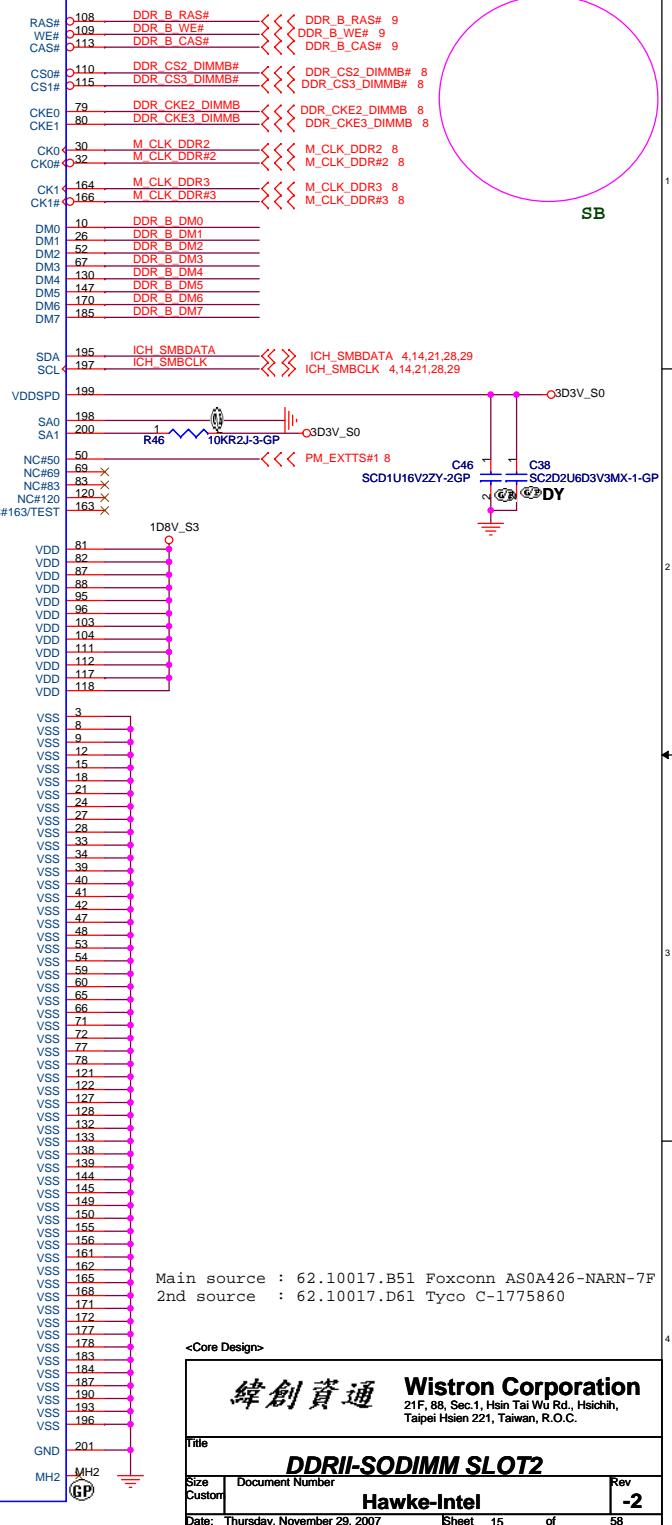
DDR_B_MA0 102
DDR_B_MA1 101
DDR_B_MA2 100
DDR_B_MA3 99
DDR_B_MA4 98
DDR_B_MA5 97
DDR_B_MA6 96
DDR_B_MA7 95
DDR_B_MA8 94
DDR_B_MA9 93
DDR_B_MA10 92
DDR_B_MA11 91
DDR_B_MA12 90
DDR_B_MA13 89
DDR_B_MA14 88
DDR_B_BS2 87
DDR_B_BS1 86
DDR_B_BS0 85
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
A14
A15
A16/BA2

DDR_B_D0 5
DDR_B_D1 7
DDR_B_D2 17
DDR_B_D3 19
DDR_B_D4 19
DDR_B_D5 6
DDR_B_D6 14
DDR_B_D7 16
DDR_B_D8 23
DDR_B_D9 25
DDR_B_D10 35
DDR_B_D11 37
DDR_B_D12 20
DDR_B_D13 22
DDR_B_D14 36
DDR_B_D15 38
DDR_B_D16 43
DDR_B_D17 45
DDR_B_D18 55
DDR_B_D19 44
DDR_B_D20 57
DDR_B_D21 46
DDR_B_D22 56
DDR_B_D23 58
DDR_B_D24 61
DDR_B_D25 63
DDR_B_D26 73
DDR_B_D27 75
DDR_B_D28 62
DDR_B_D29 64
DDR_B_D30 74
DDR_B_D31 76
DDR_B_D32 123
DDR_B_D33 125
DDR_B_D34 135
DDR_B_D35 137
DDR_B_D36 124
DDR_B_D37 126
DDR_B_D38 134
DDR_B_D39 136
DDR_B_D40 141
DDR_B_D41 143
DDR_B_D42 151
DDR_B_D43 153
DDR_B_D44 140
DDR_B_D45 142
DDR_B_D46 152
DDR_B_D47 154
DDR_B_D48 157
DDR_B_D49 159
DDR_B_D50 173
DDR_B_D51 175
DDR_B_D52 158
DDR_B_D53 160
DDR_B_D54 174
DDR_B_D55 176
DDR_B_D56 179
DDR_B_D57 181
DDR_B_D58 189
DDR_B_D59 191
DDR_B_D60 180
DDR_B_D61 182
DDR_B_D62 192
DDR_B_D63 194

DDR_B_DQS#0 11
DDR_B_DQS#1 25
DDR_B_DQS#2 49
DDR_B_DQS#3 68
DDR_B_DQS#4 129
DDR_B_DQS#5 146
DDR_B_DQS#6 167
DDR_B_DQS#7 186
DDR_B_DQS0 13
DDR_B_DQS1 31
DDR_B_DQS2 51
DDR_B_DQS3 70
DDR_B_DQS4 131
DDR_B_DQS5 148
DDR_B_DQS6 169
DDR_B_DQS7 188
DQS0#
DQS1#
DQS2#
DQS3#
DQS4#
DQS5#
DQS6#
DQS7#

DDR_B_DQS0 13
DDR_B_DQS1 31
DDR_B_DQS2 51
DDR_B_DQS3 70
DDR_B_DQS4 131
DDR_B_DQS5 148
DDR_B_DQS6 169
DDR_B_DQS7 188
OTD0
OTD1
VREF
VSS
GND
MH1
MH2

REVERSE TYPE High 9.2 mm



Main source : 62.10017.B51 Foxconn AS0A426-NARN-7F
2nd source : 62.10017.D61 Tyco C-1775860

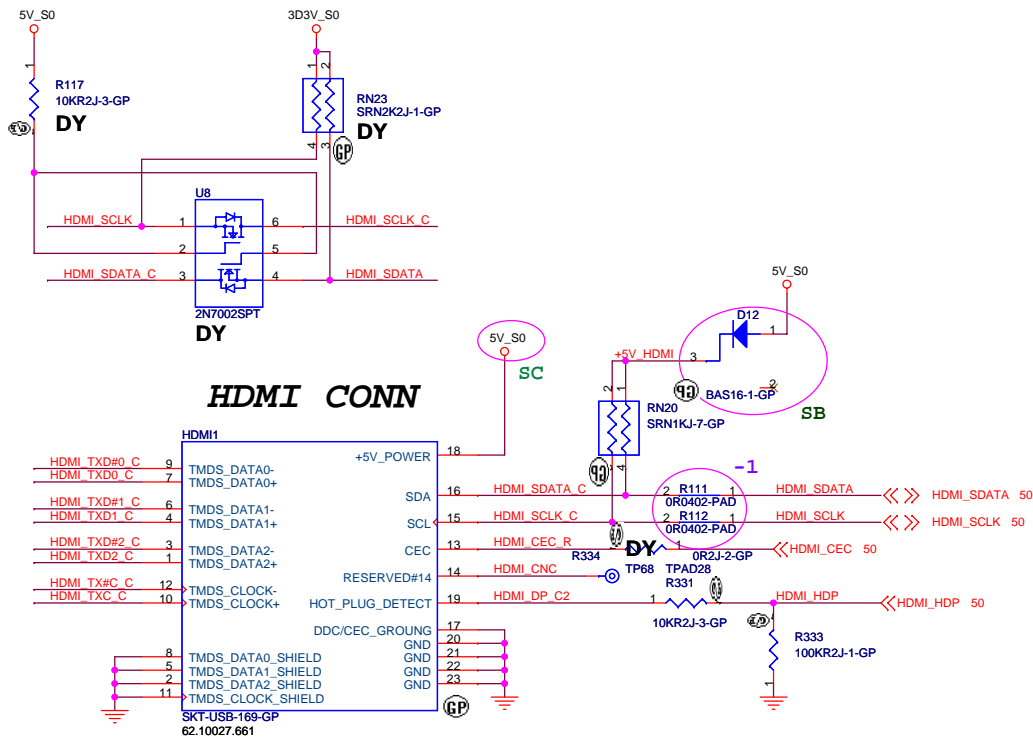
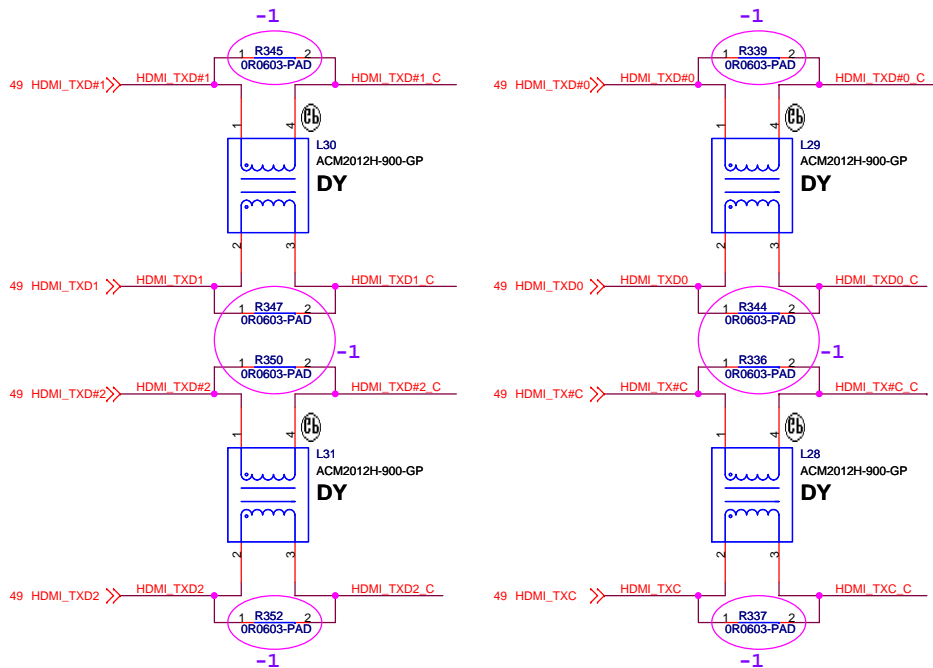
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Size Custom Document Number
Date: Thursday, November 29, 2007 Sheet 15 of 58

DDR2-SODIMM SLOT2
Hawke-Intel
-2

HDMI I/F & CONNECTOR



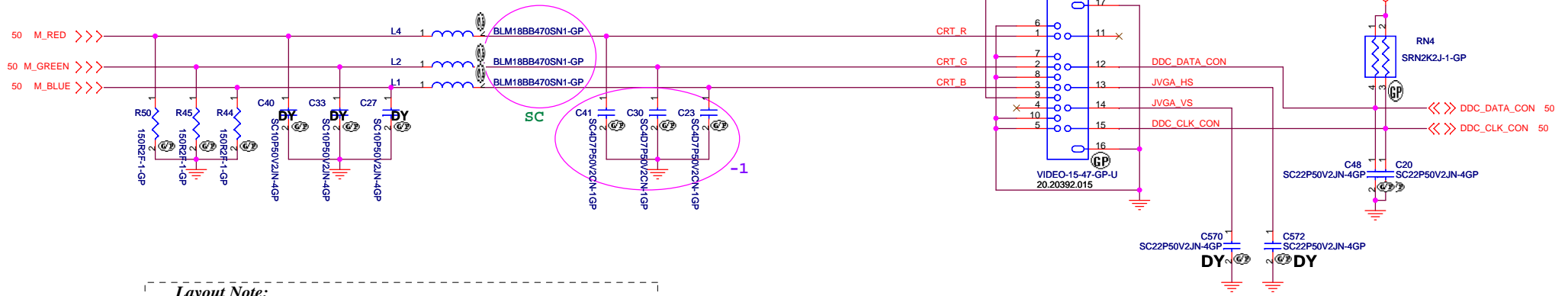
Main source : 62.10027.661 Molex 47408-0201
2nd source : 62.10078.121 Tyco C1759548-1

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

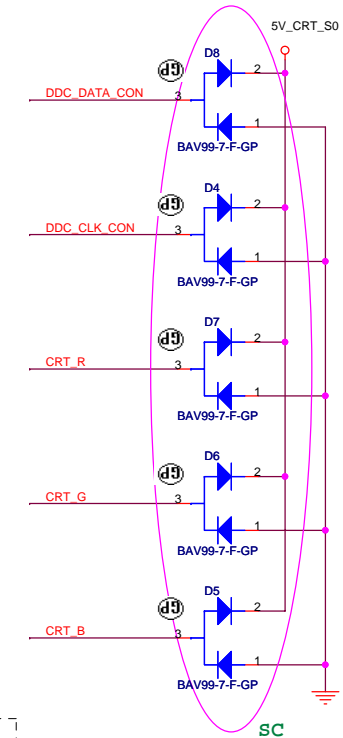
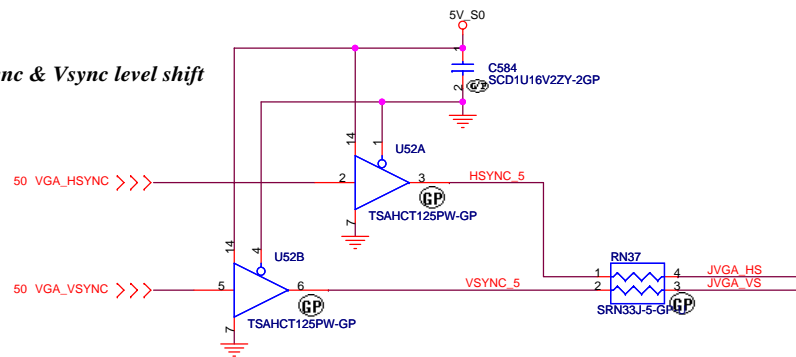
Title			HDMI	
Size A3	Document Number	Hawke-Intel		Rev
Date: Thursday, November 22, 2007		Sheet 16	of 58	-2

CRT I/F & CONNECTOR



Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



TP28-75-GP	TP177	5V_CRT_S0
TP28-75-GP	TP176	DDC_DATA_CON
TP28-75-GP	TP179	DDC_CLK_CON
TP28-75-GP	TP178	CRT_R
TP28-75-GP	TP180	CRT_G
TP28-75-GP	TP182	CRT_B
TP28-75-GP	TP181	JPGA_HS
TP28-75-GP	TP183	JPGA_VS

For AFTE, place them on the same side.

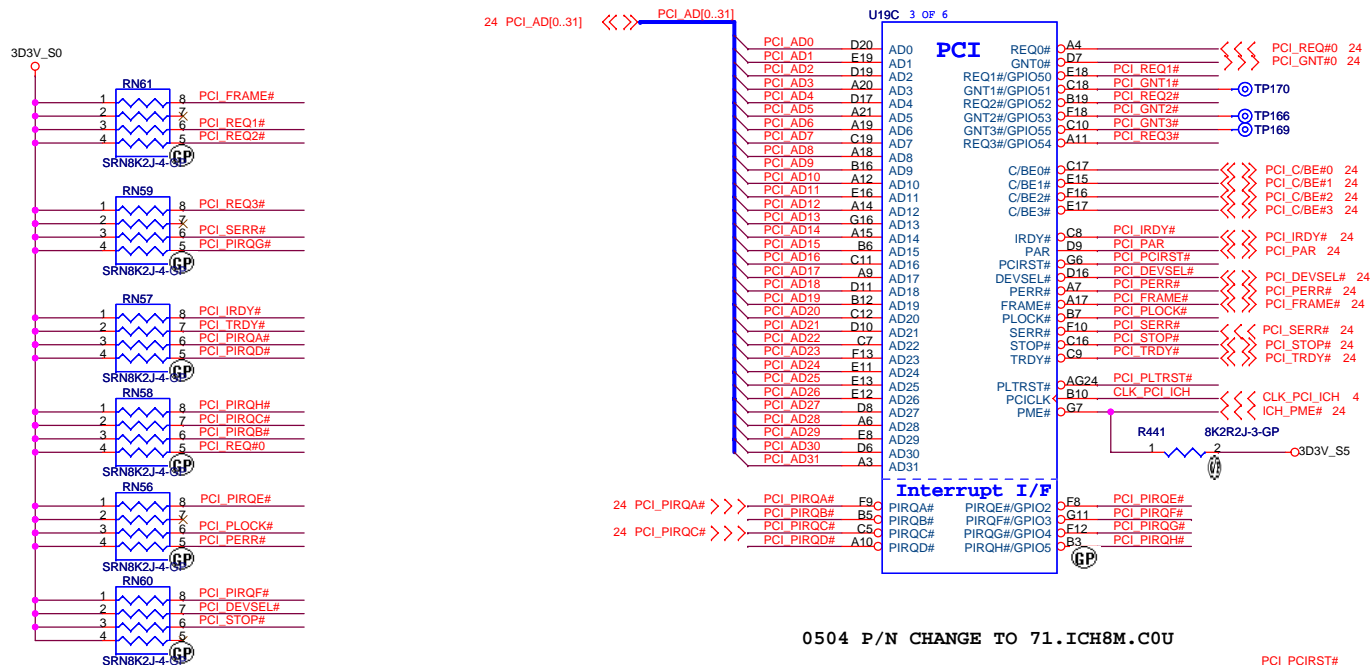
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector	
Size A3	Document Number	Rev
	Hawke-Intel	-2
Date: Thursday, November 22, 2007	Sheet 17	of 58

PCI Interface Routing

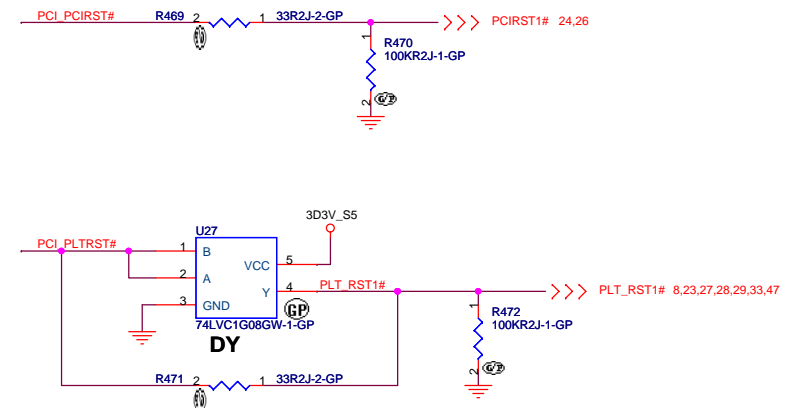
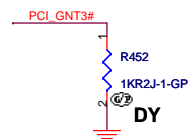
	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A C	0	0



ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

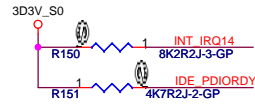
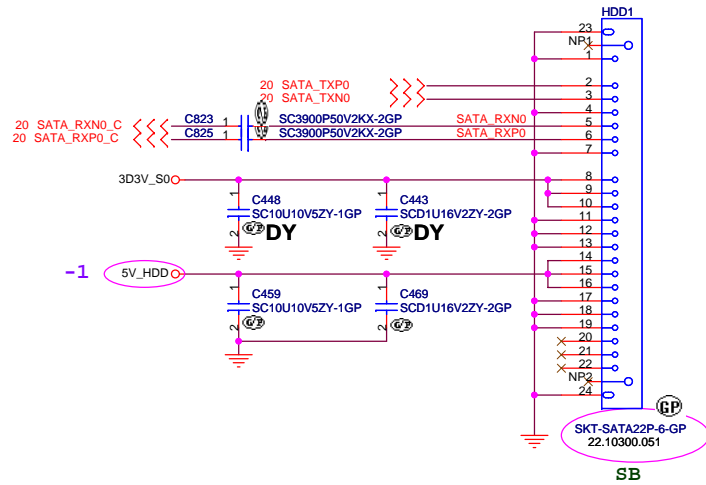


<Core Design>

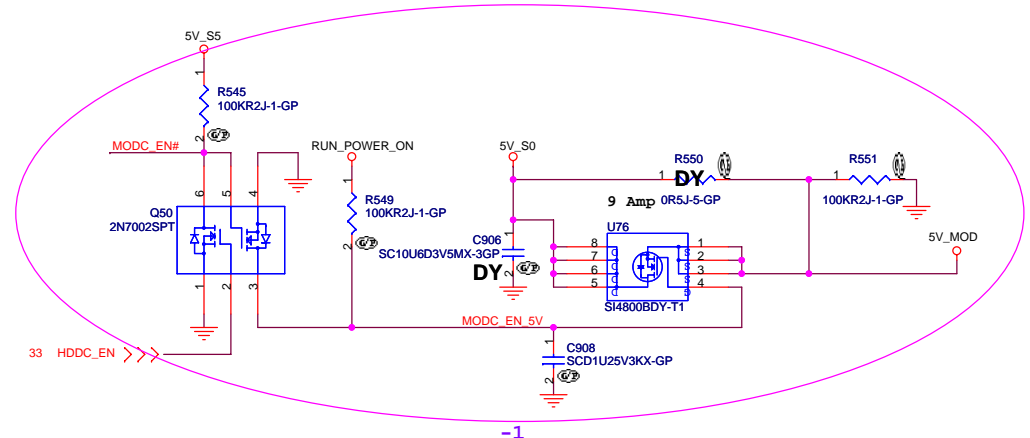
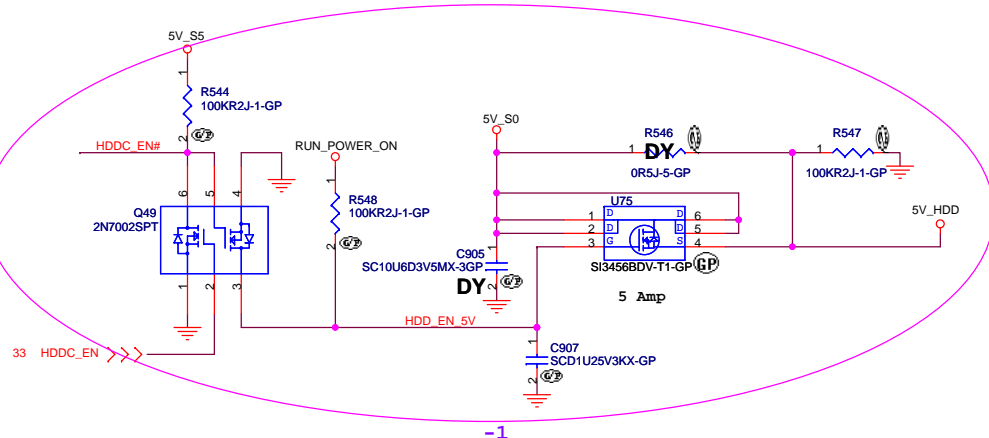
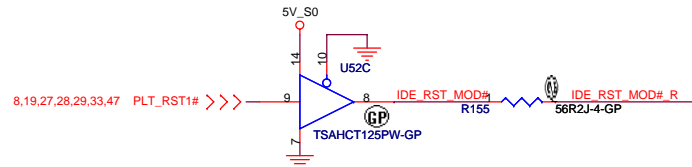
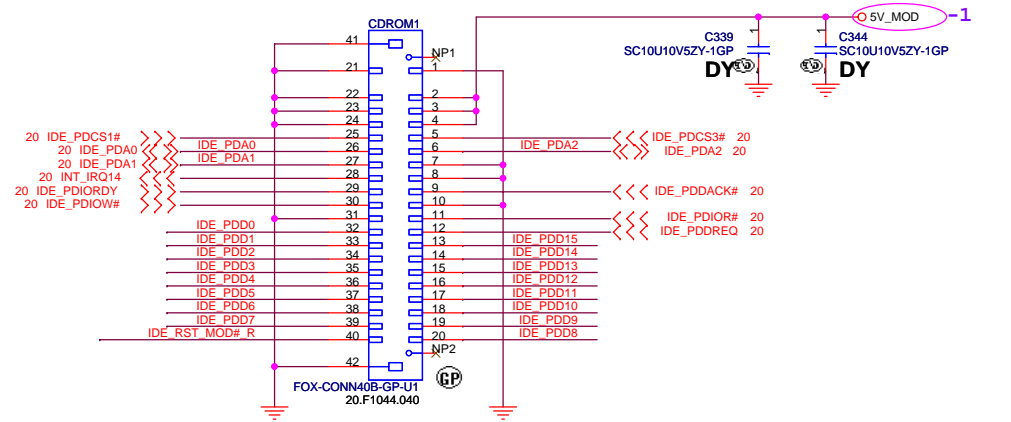
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH8(1/4)-PCI/INT		
Size A3	Document Number	Hawke-Intel	Rev -2
Date: Thursday, November 22, 2007	Sheet 19	of 58	

SATA HDD Connector



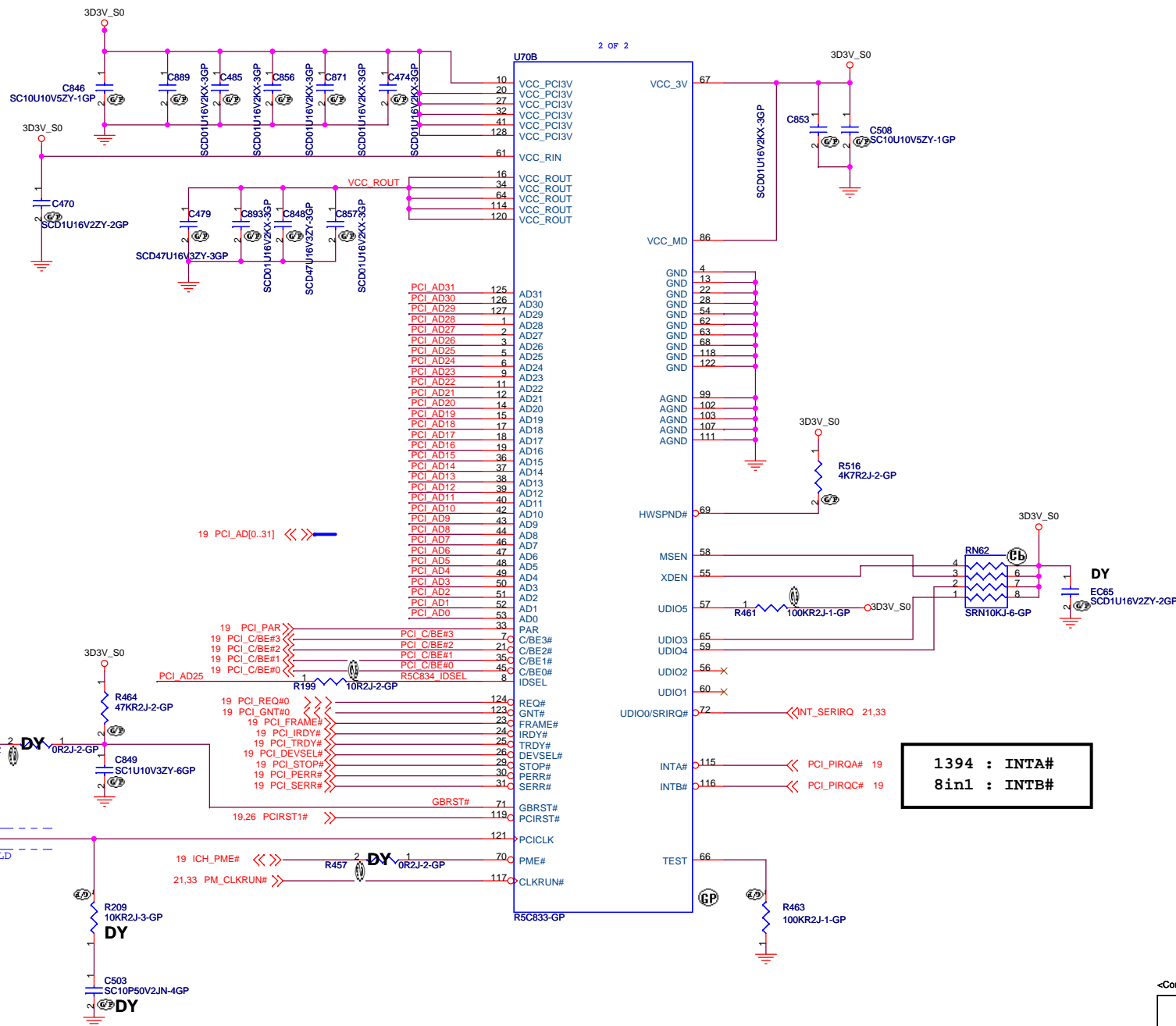
ODD Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File	HDD/ODD		
Size	Document Number	Hawke-Intel	Rev -2
A3	Date: Thursday, November 22, 2007	Sheet 23 of 58	

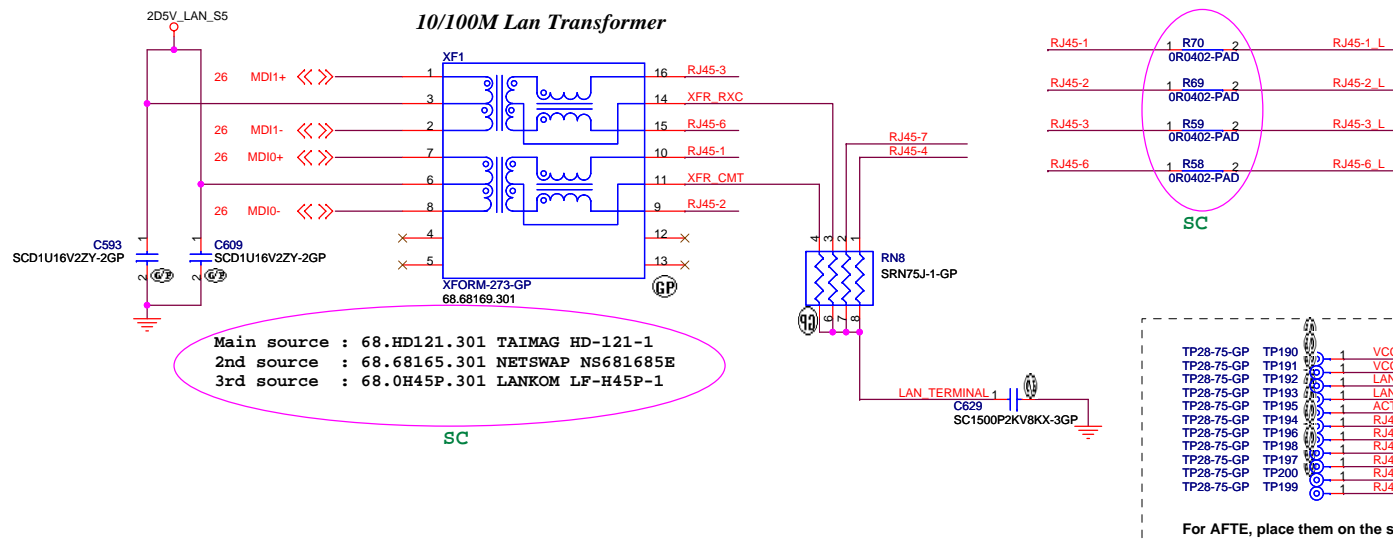


<Core Design>

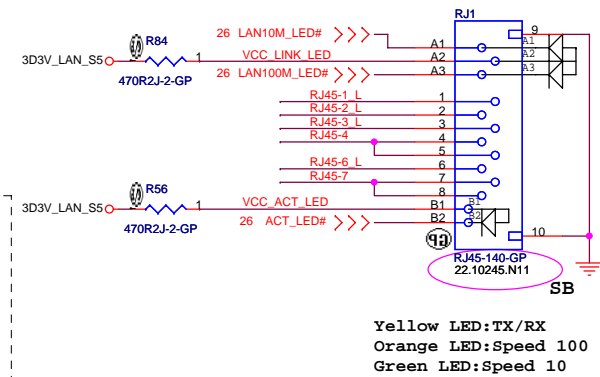
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
R5C833/PCI		
Size	Document Number	Rev
A3	Hawke-Intel	-2
Date:	Thursday, November 22, 2007	Sheet 24 of 58

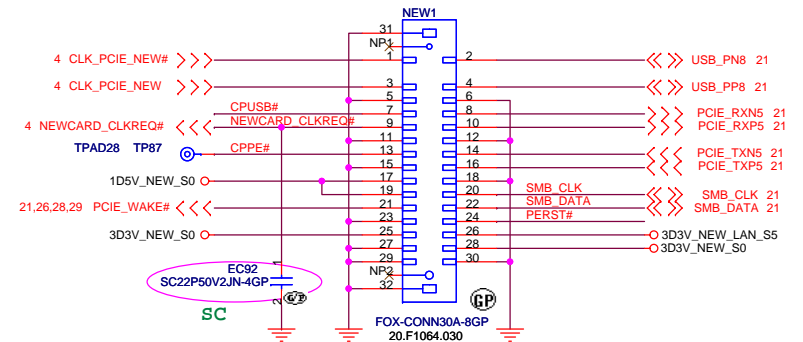
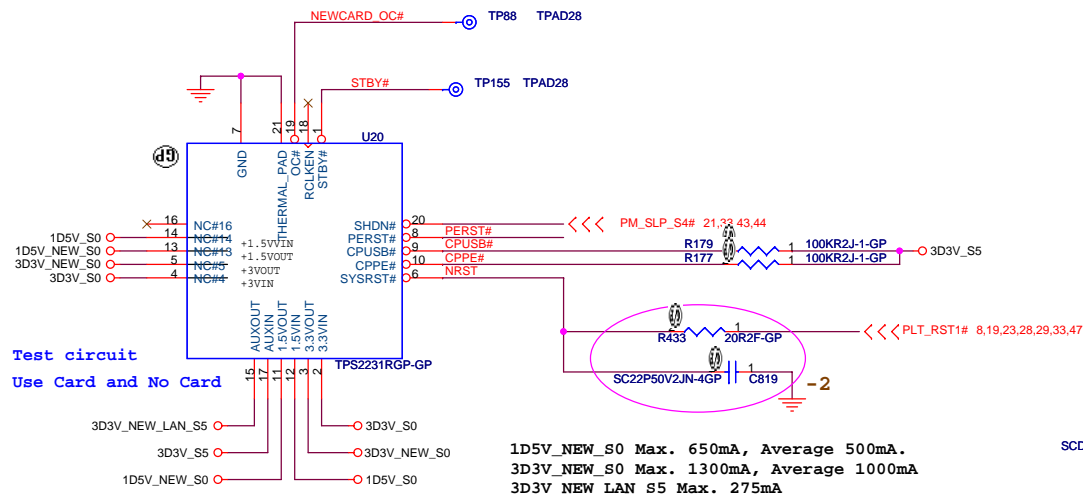
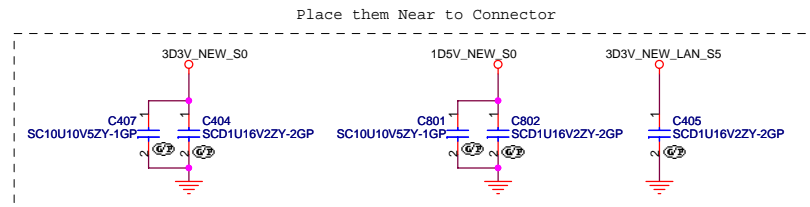
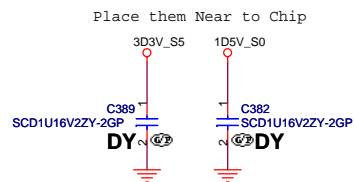
RJ45 Connector



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



NEWCARD Connector



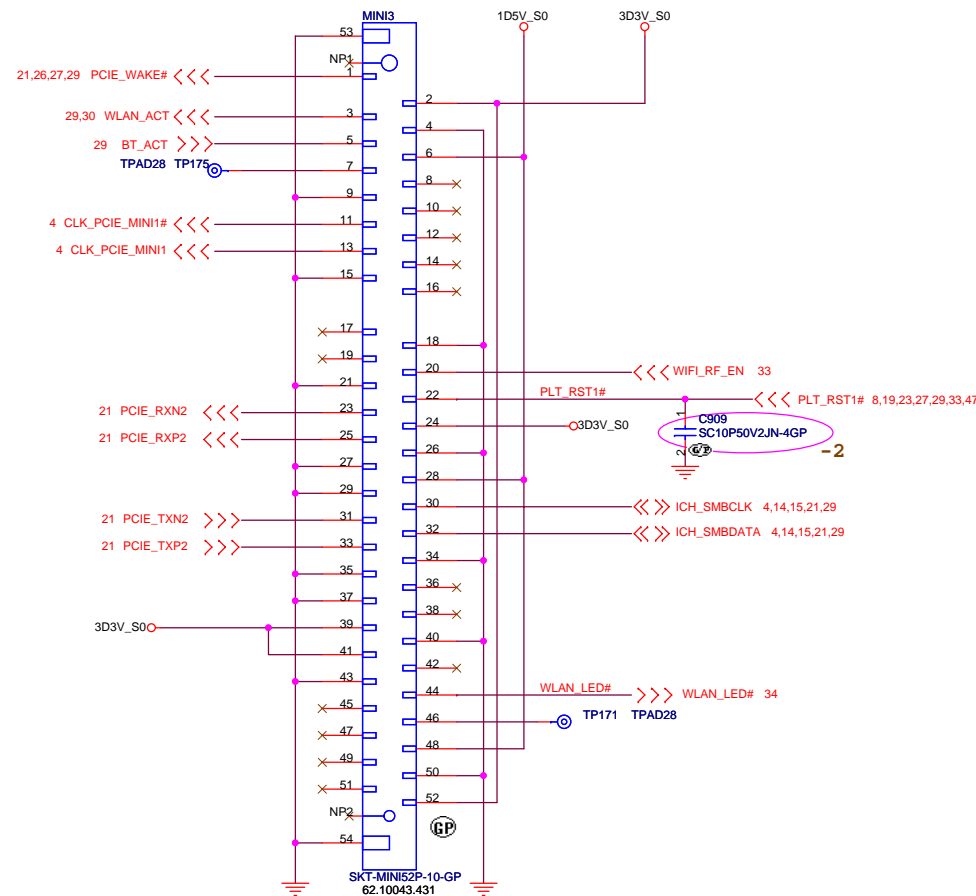
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

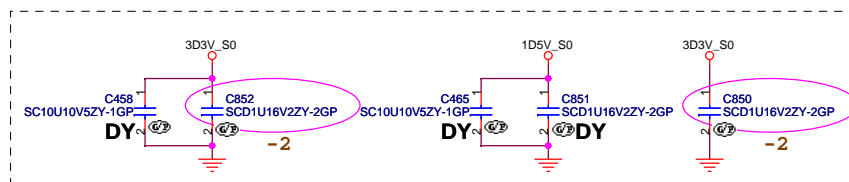
Title		
LAN connector/NEW CARD		
Size	Document Number	Rev
A3	Hawke-Intel	-2
Date:	Thursday, November 22, 2007	Sheet 27 of 58

www.vinafix.vn

Mini Card Connector 1(802.11a/b/g)

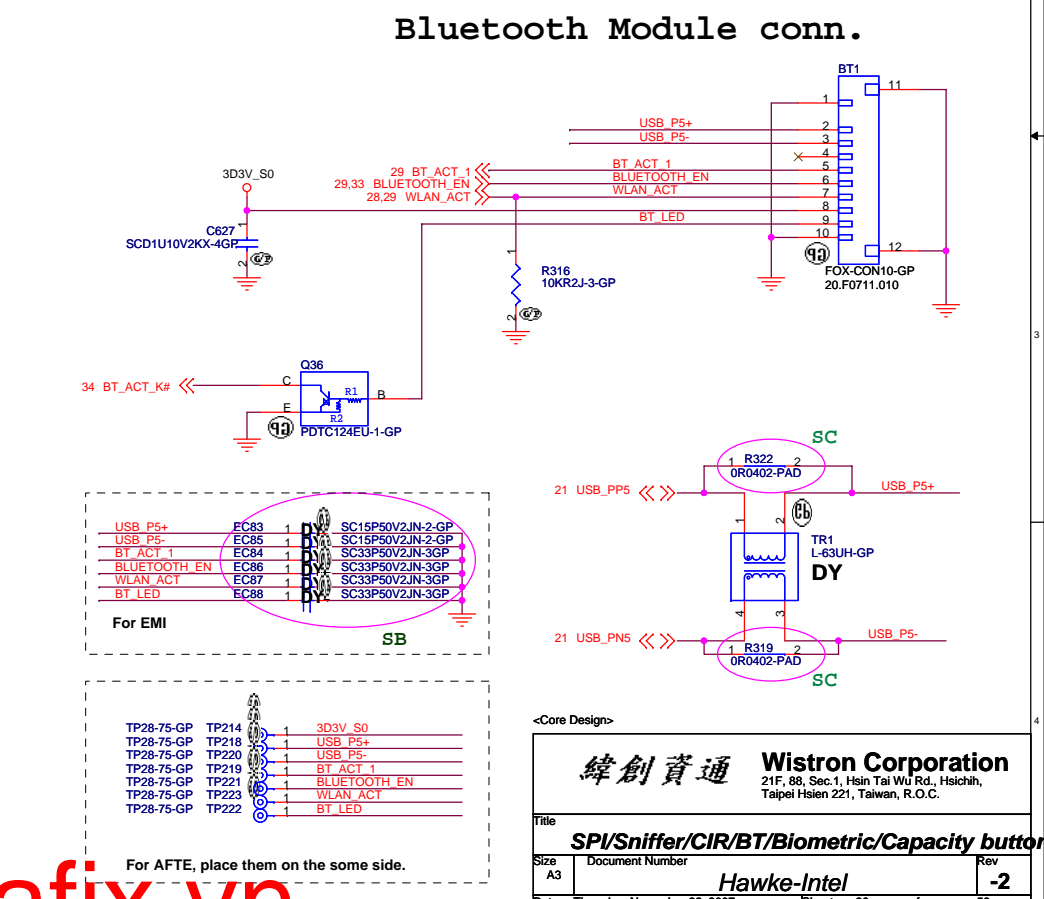
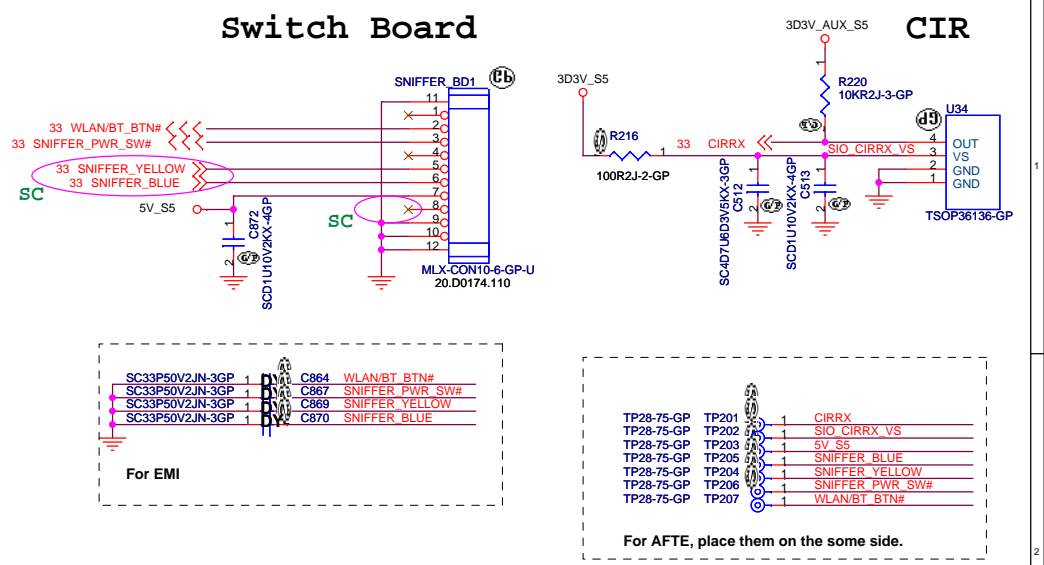
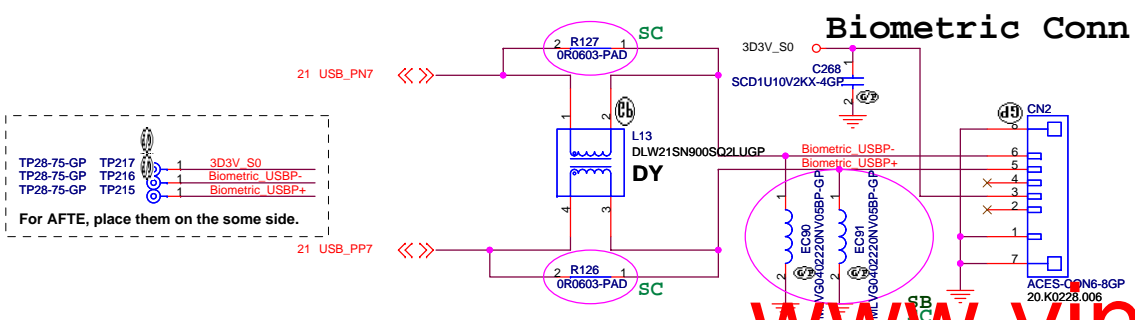
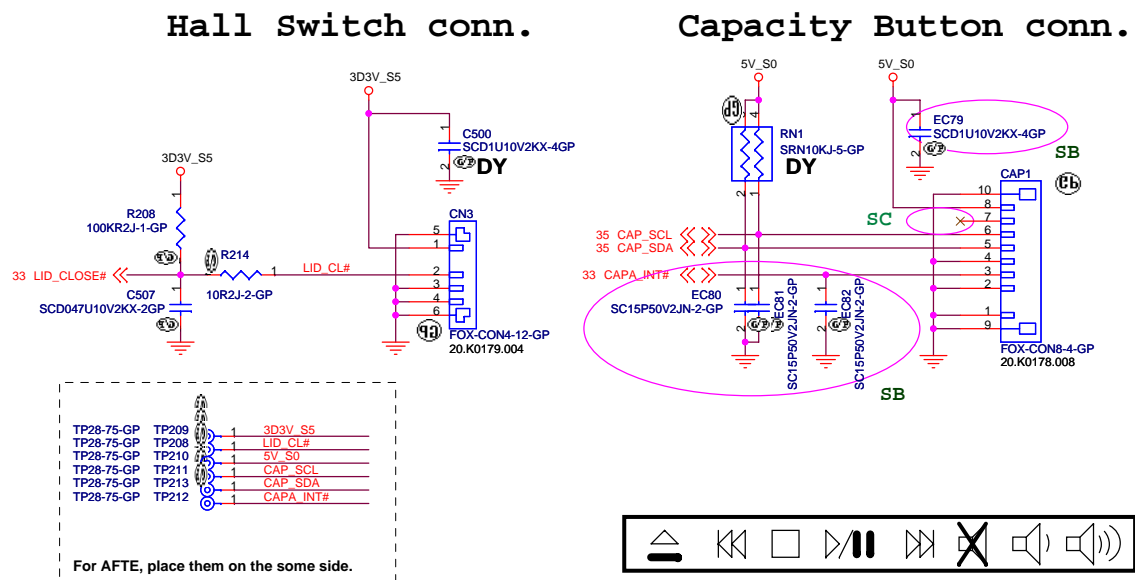
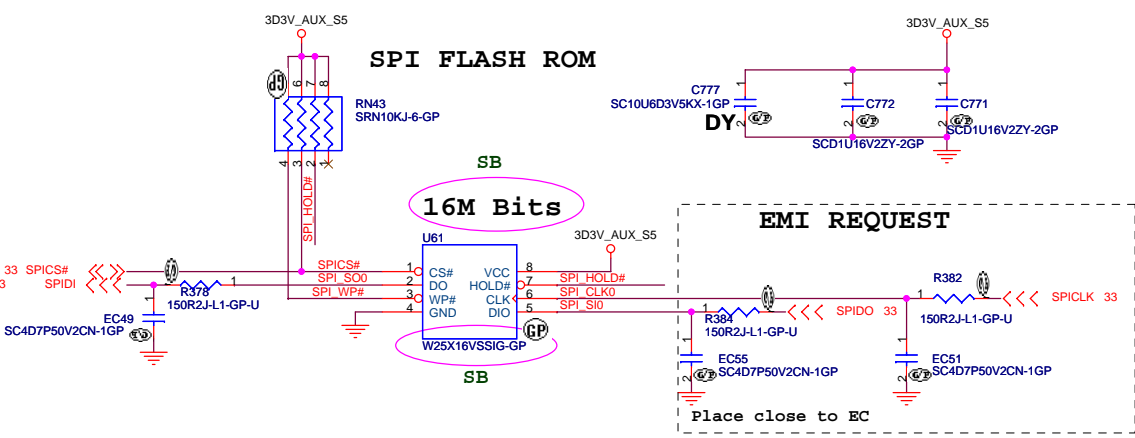


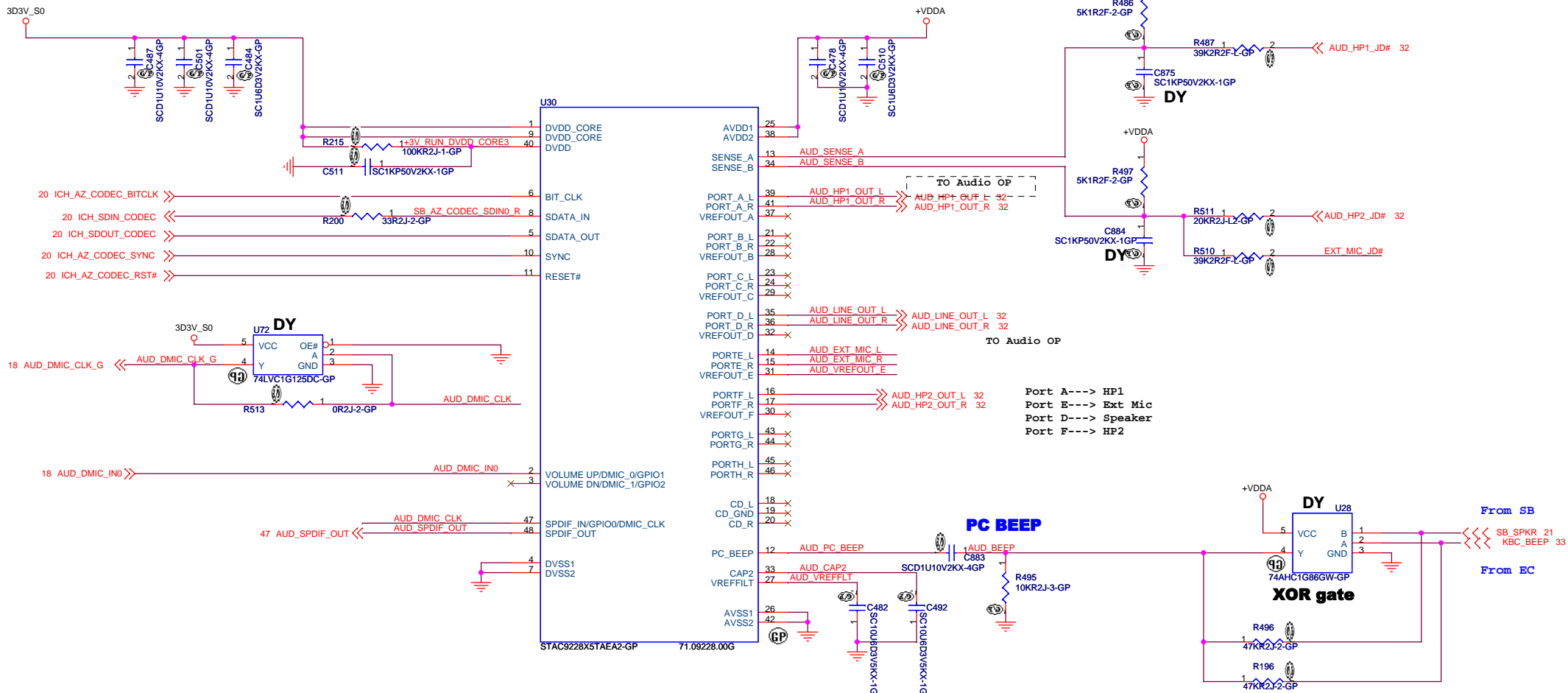
Main source : 20.F0992.052 P-Two A54452-A0G16-N
2nd source : 62.10043.551 Tyco 1759553-1



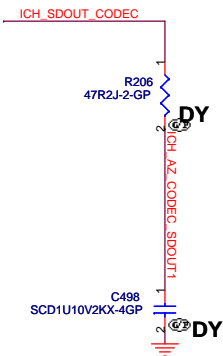
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MINI CARD CONN 1	
Size A3	Document Number
Hawke-Intel	
Date: Thursday, November 22, 2007	Sheet 28 of 58
Rev -2	

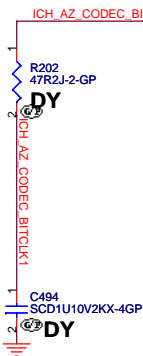




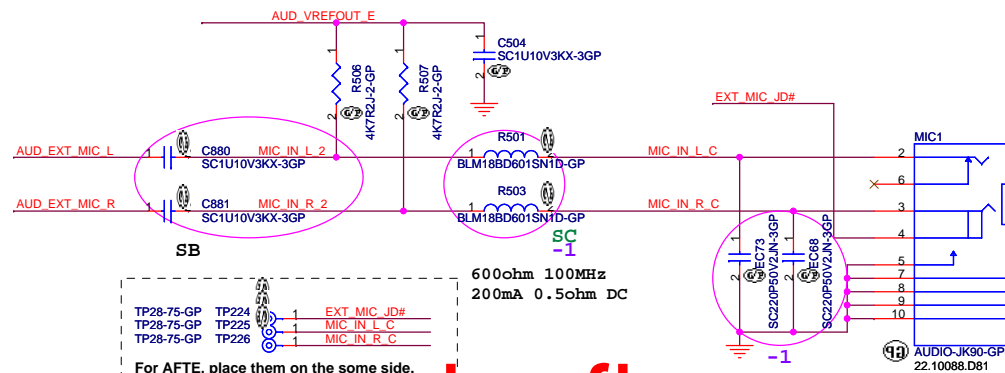
Azalia I/F EMI



Azalia I/F EMI



MIC IN



<Core Design>

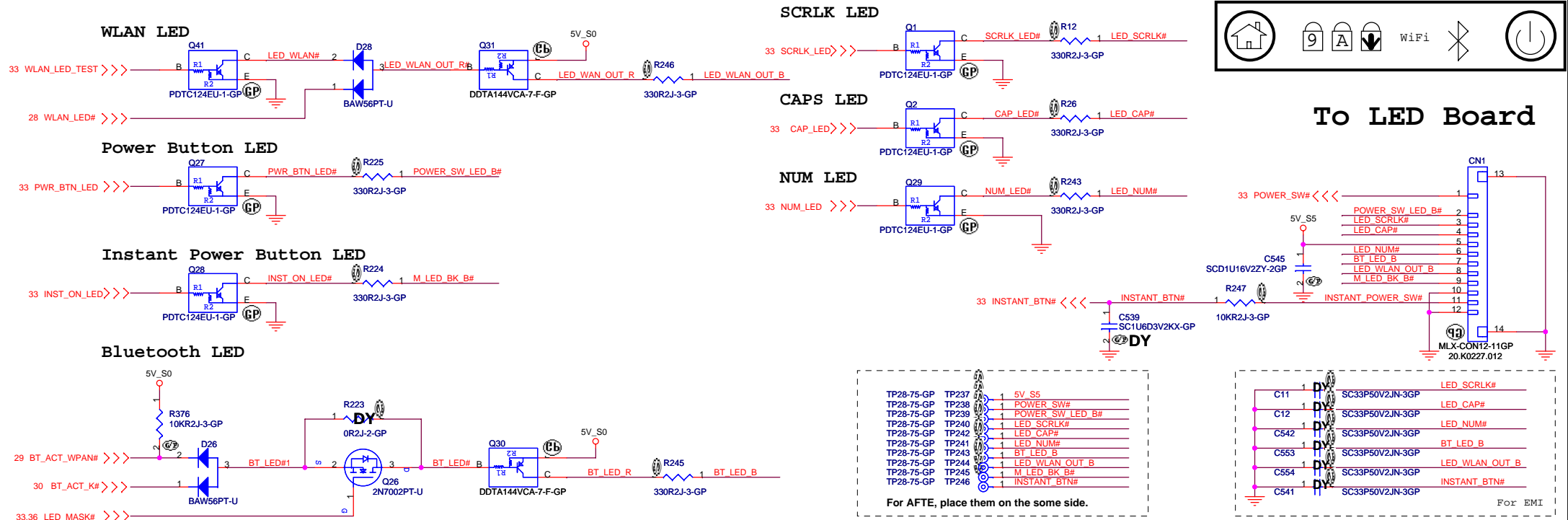
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **AUDIO CODEC STAC9228**

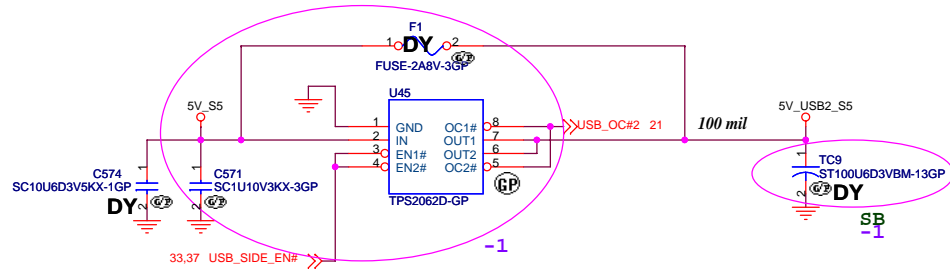
Size A3 Document Number **Hawke-Intel** Rev **-2**

Date: Thursday, November 22, 2007 Sheet 31 of 58

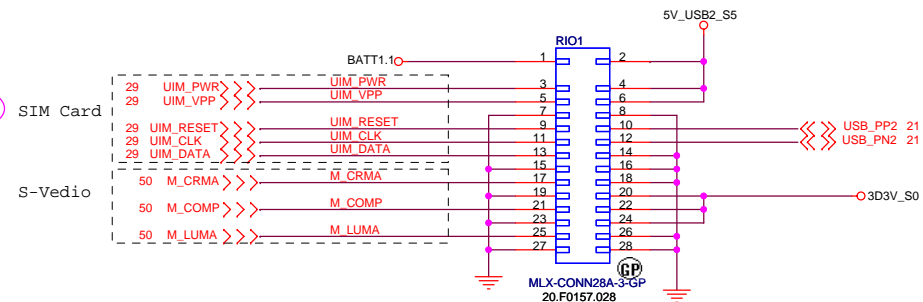
www.vinafix.vn

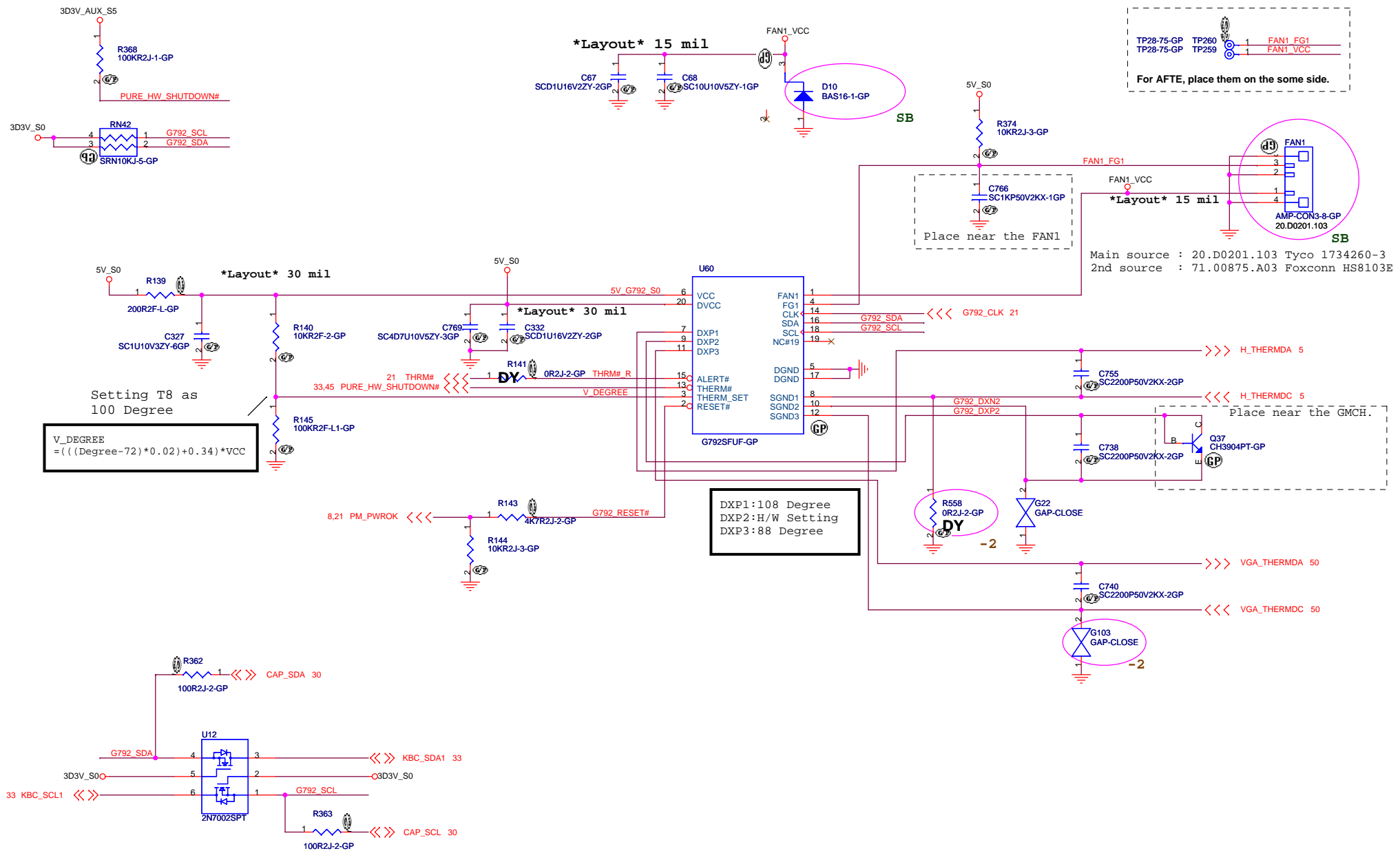


USB POWER



To Right I/O Board



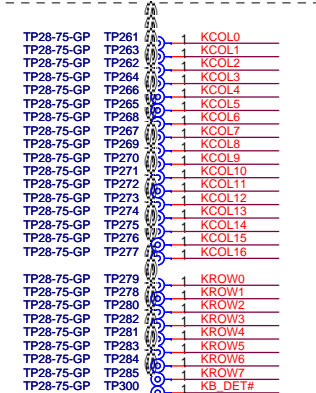
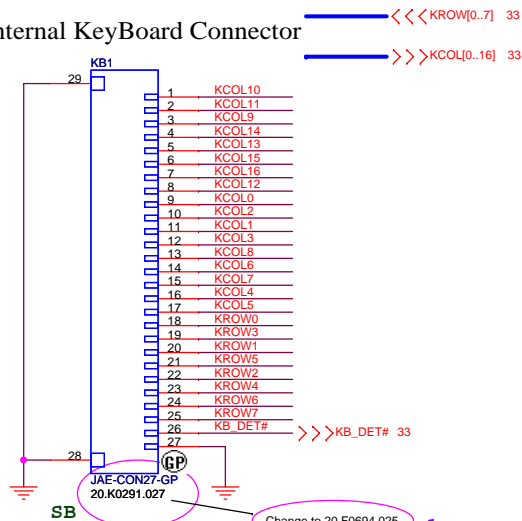


<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

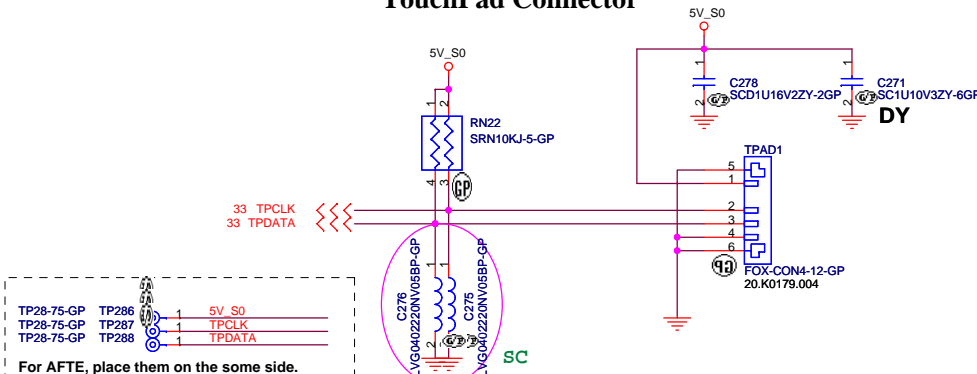
Title			Thermal/Fan Contrllor G792	
Size	Document Number	Hawke-Intel		Rev
A3				-2
Date:	Thursday, November 22, 2007	Sheet	35	of 58

Internal Keyboard Connector



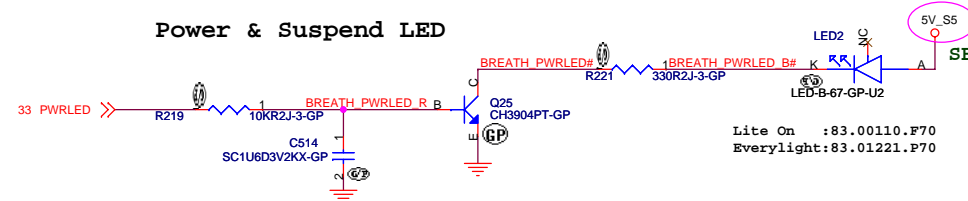
For AFTE, place them on the same side.

TouchPad Connector



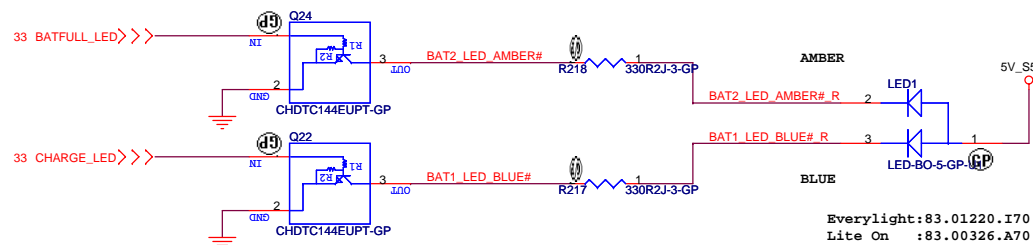
For AFTE, place them on the same side.

Power & Suspend LED



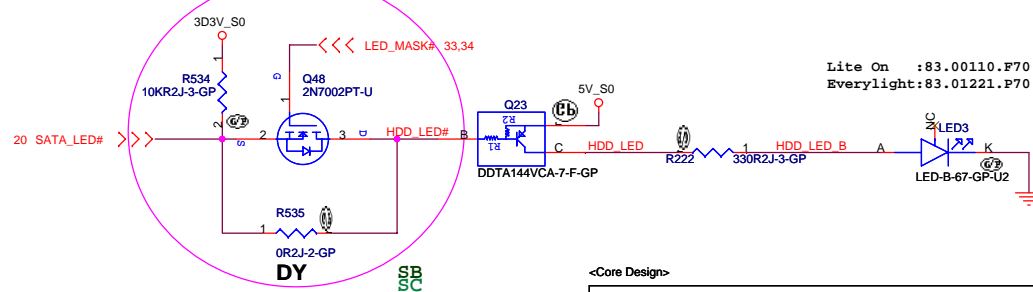
Lite On :83.00110.F70
Everylight:83.01221.P70

Battery LED



Everylight:83.01220.I70
Lite On :83.00326.A70

HDD LED



Lite On :83.00110.F70
Everylight:83.01221.P70

LED NAME

ACTIVE SIGNAL

Power Button LED	PWR_BTN_LED	*
Instant Power Button LED	INST_ON_LED	*
WLAN LED	WLAN_LED_TEST (from KBC) WLAN_LED# (from Mini)	
Bluetooth LED	BT_ACT_WPAN# (from Mini) BT_ACT_K# (from BT)	
NUM LED	NUM_LED (from KBC)	
SCRLK LED	SCRLK_LED (from KBC)	
CAPS LED	CAP_LED (from KBC)	

LED Board

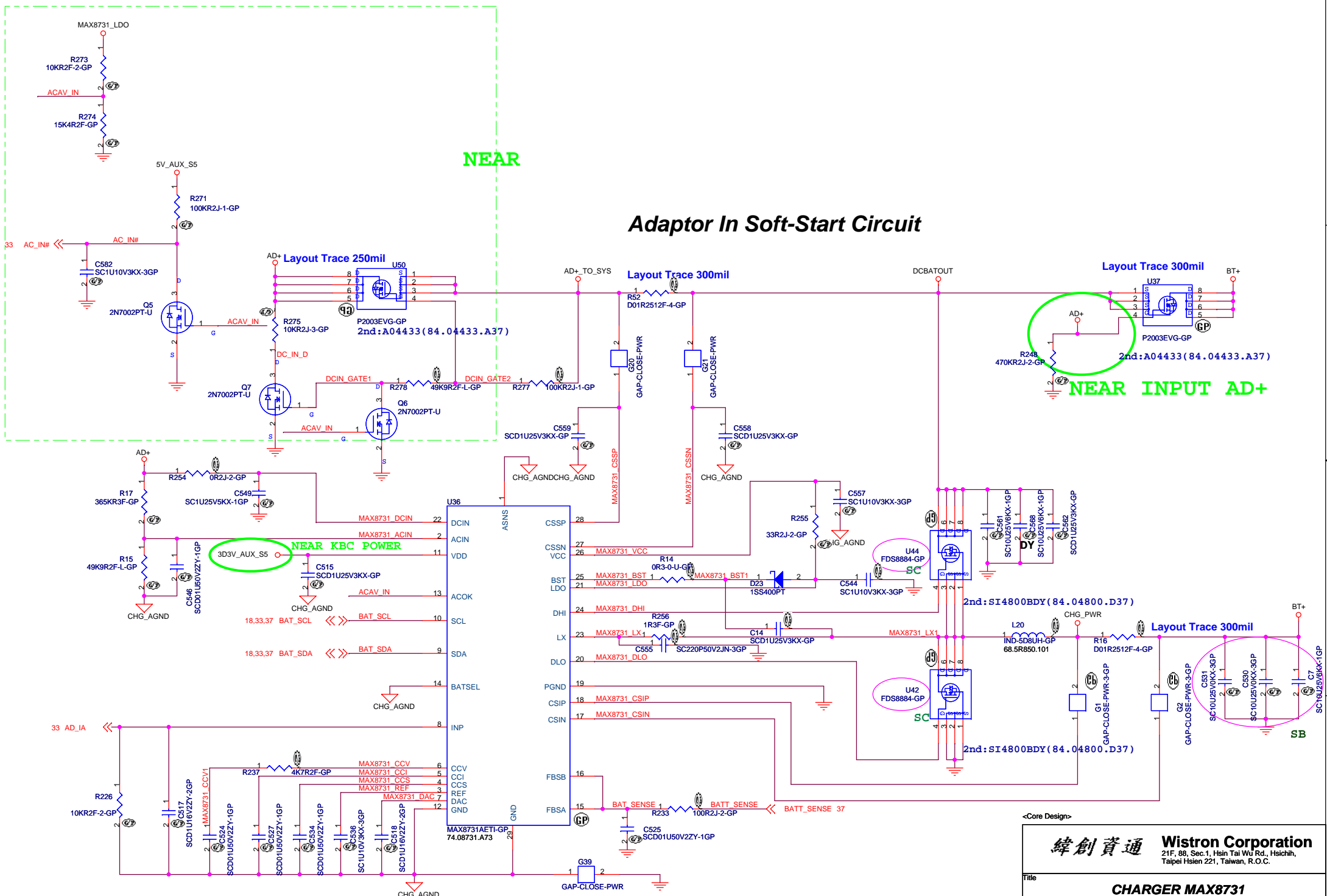
Main Board

Power & Suspend LED	PWRLED (from KBC)
HDD LED	SATA_LED# (from ICH)
Battery LED	BATFULL_LED (from KBC)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title	KeyBoard/Touchpad	Rev	-2
Size A3	Document Number	Hawke-Intel	
Date: Thursday, November 22, 2007	Sheet 36	of 58	



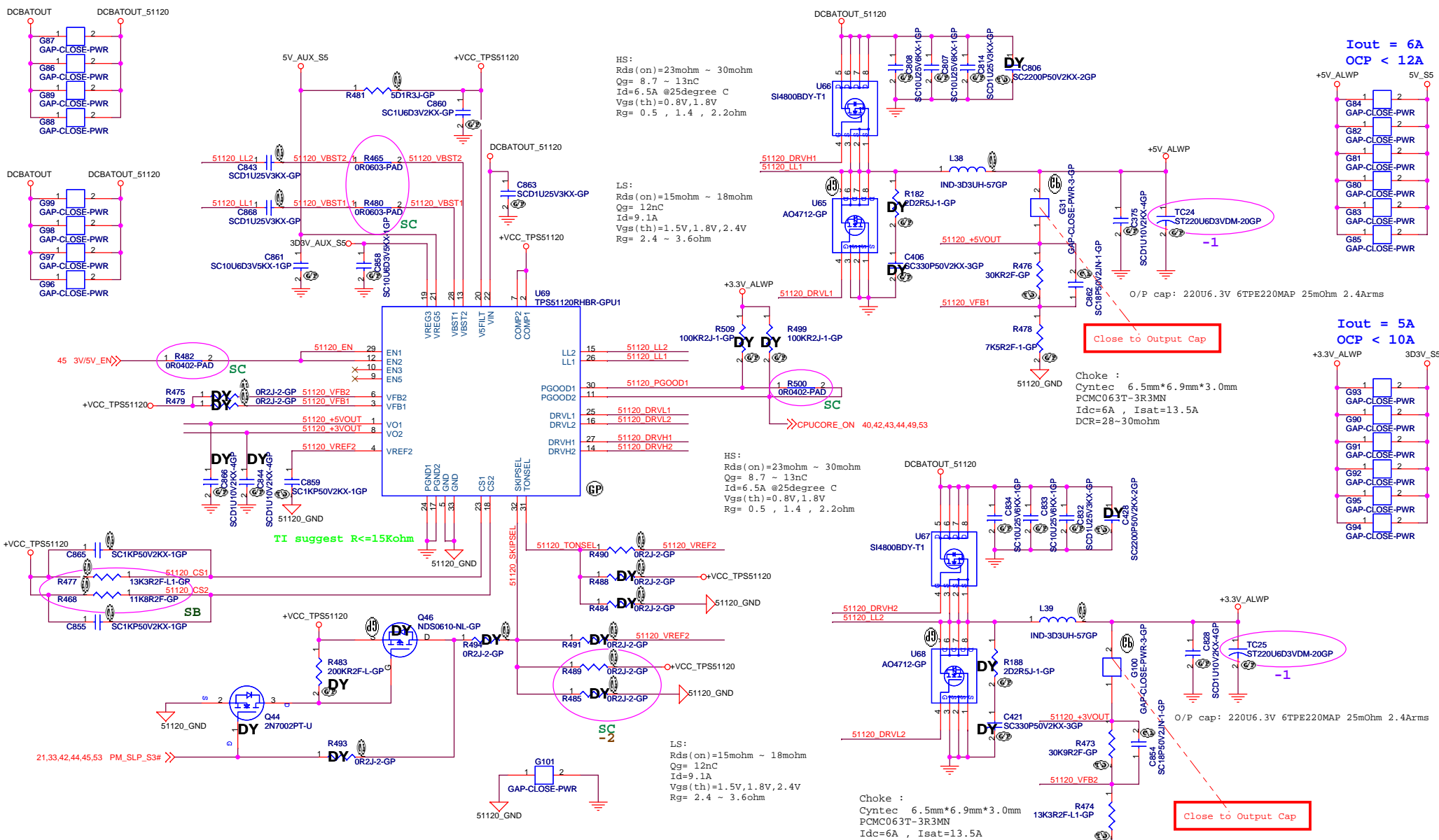
Adaptor In Soft-Start Circuit

NEAR INPUT AD+

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CHARGER MAX8731		
Size	Document Number	Rev
A3	Hawke-Intel	-2
Date:	Thursday, November 22, 2007	Sheet 38 of 58



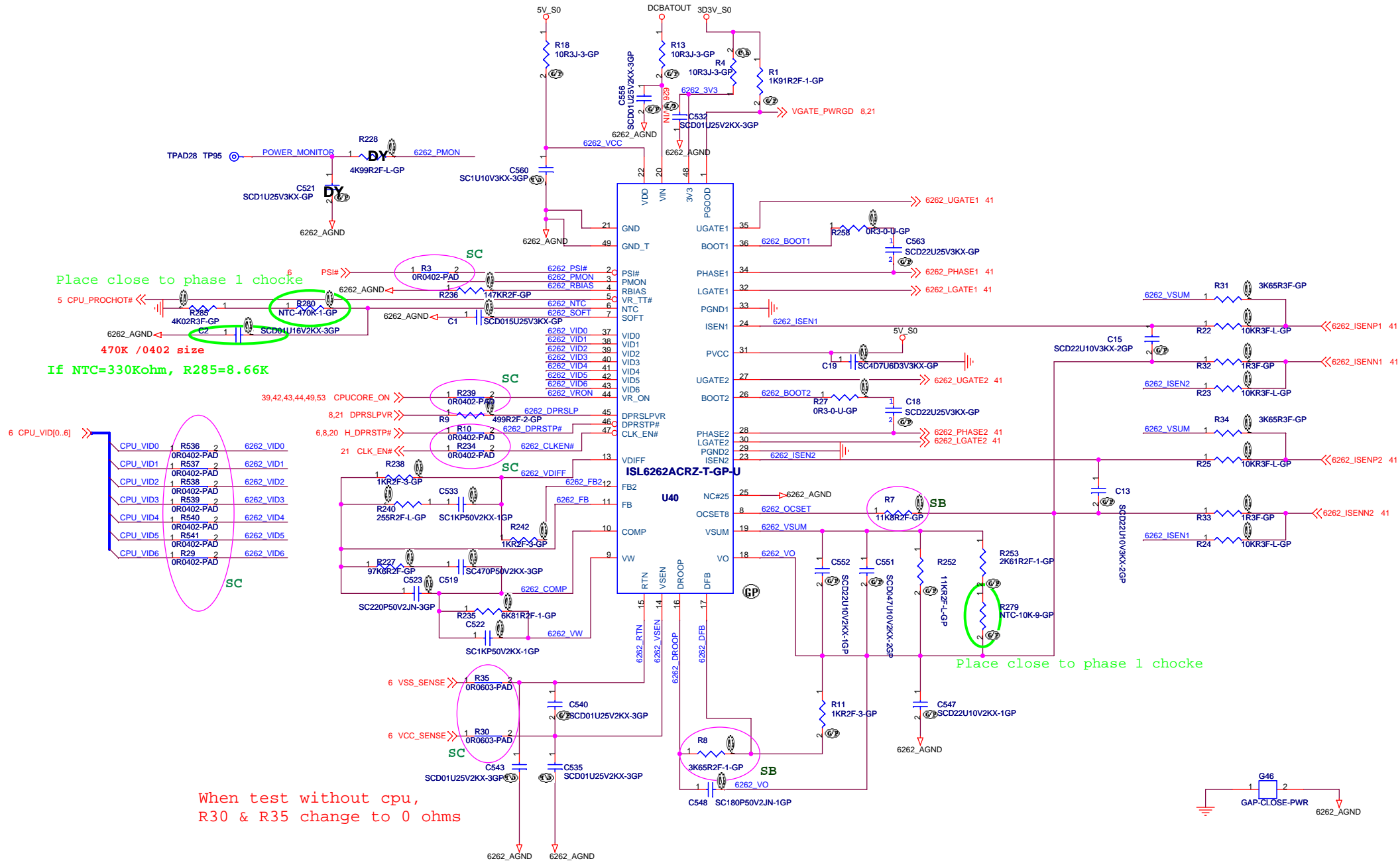
$$V_{out} = 1V \cdot (R1 + R2) / R2$$

	GND	VREF2	FLDLY	VSPILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

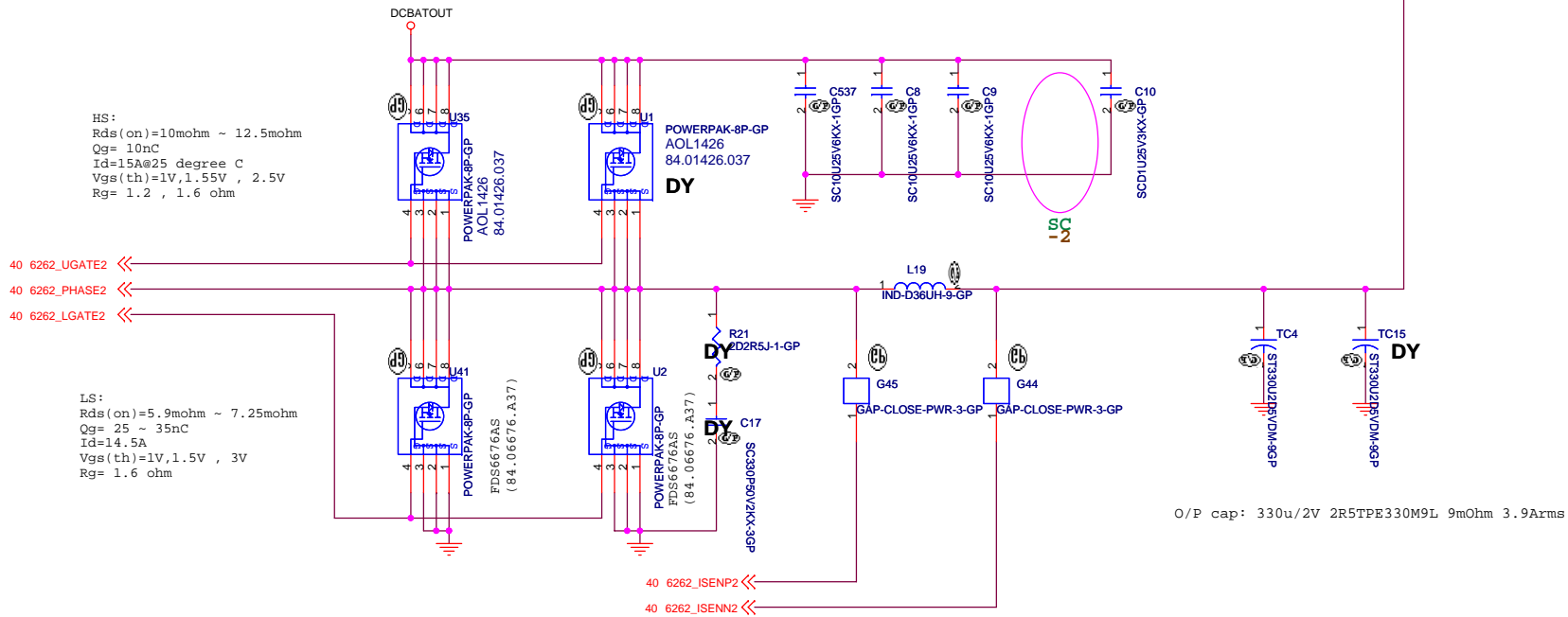
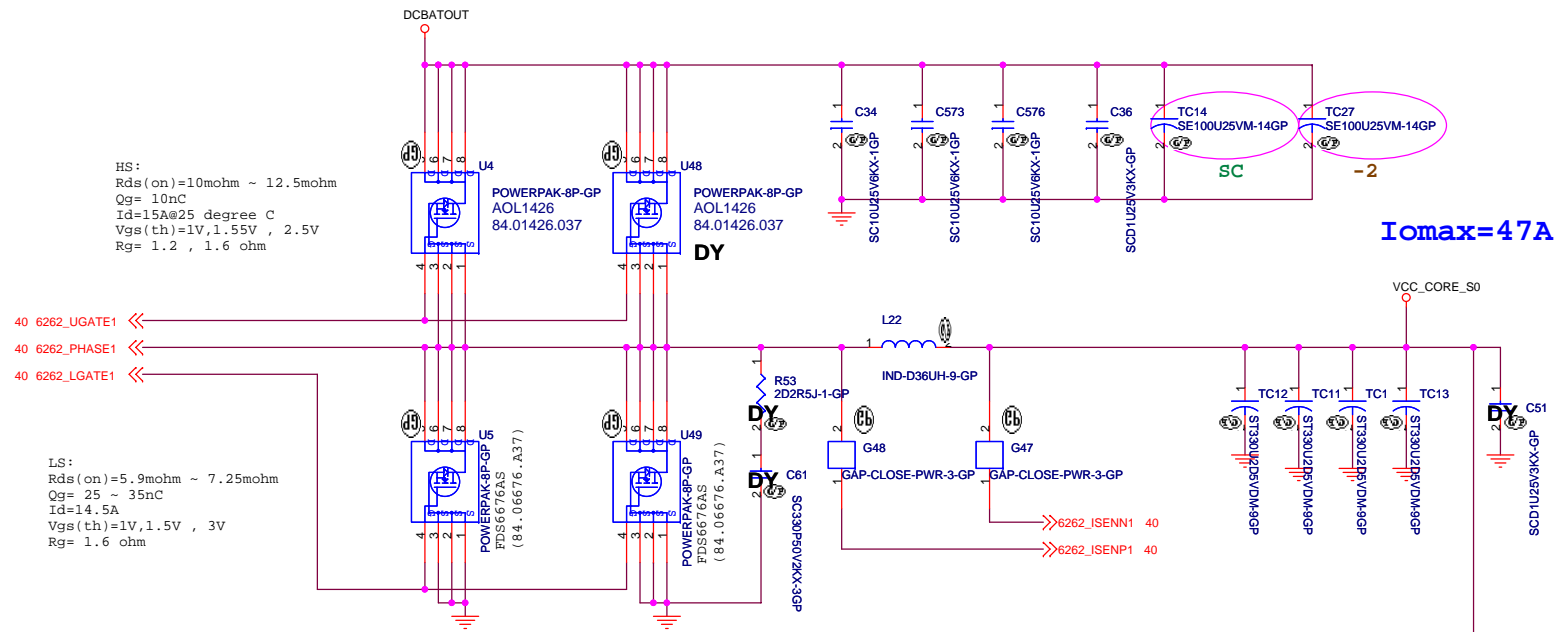
Title		DC to DC 3.3V & 5V	
Size	Document Number	Hawke-Intel	
Custpm		Rev -2	
Date:	Thursday, November 22, 2007	Sheet	39 of 58



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC-DC VCCCPUCORE 1/2			
Size	Document Number	Rev	
A3	Hawke-Intel	-2	
Date:	Thursday, November 22, 2007	Sheet	40 of 58

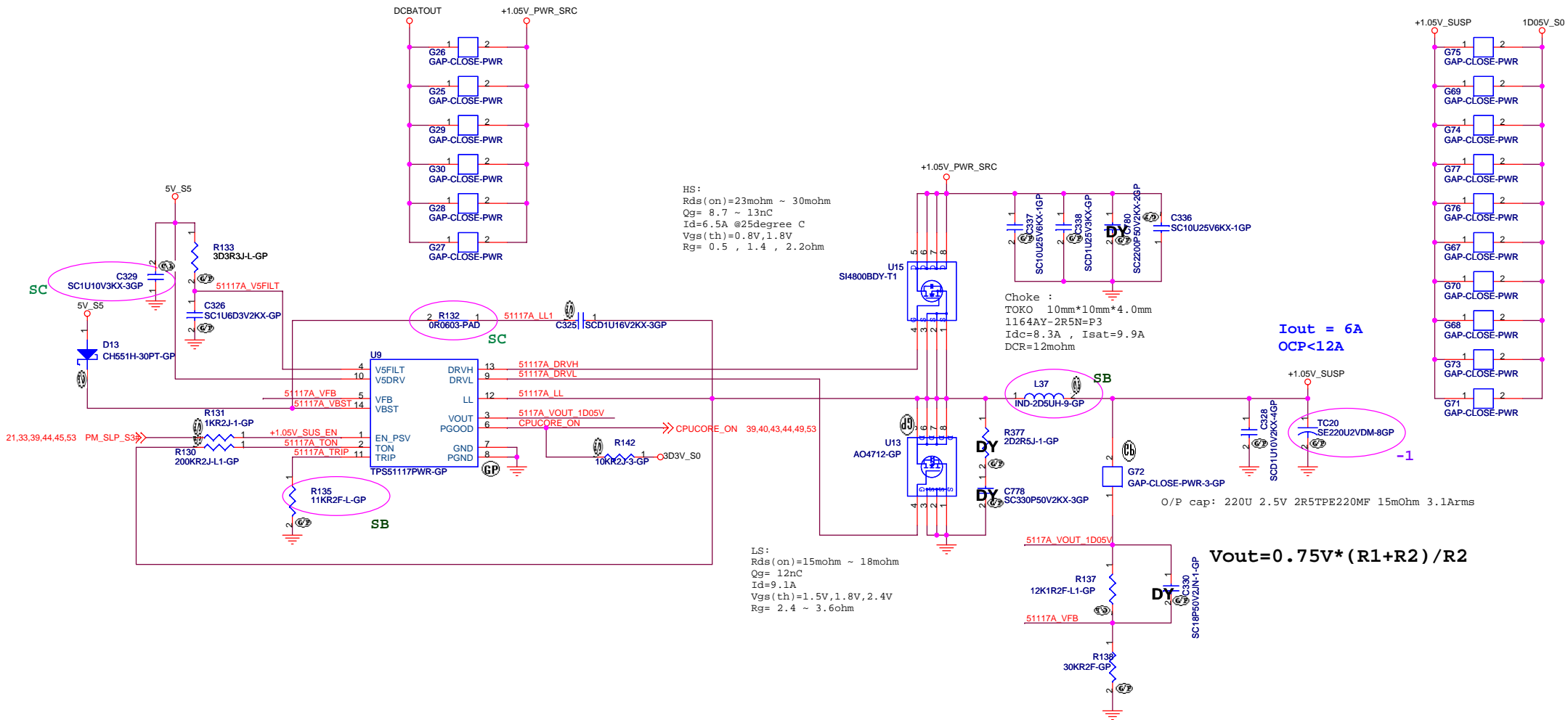


If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
 ==> Remove R44/R45/R46/R47.

<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

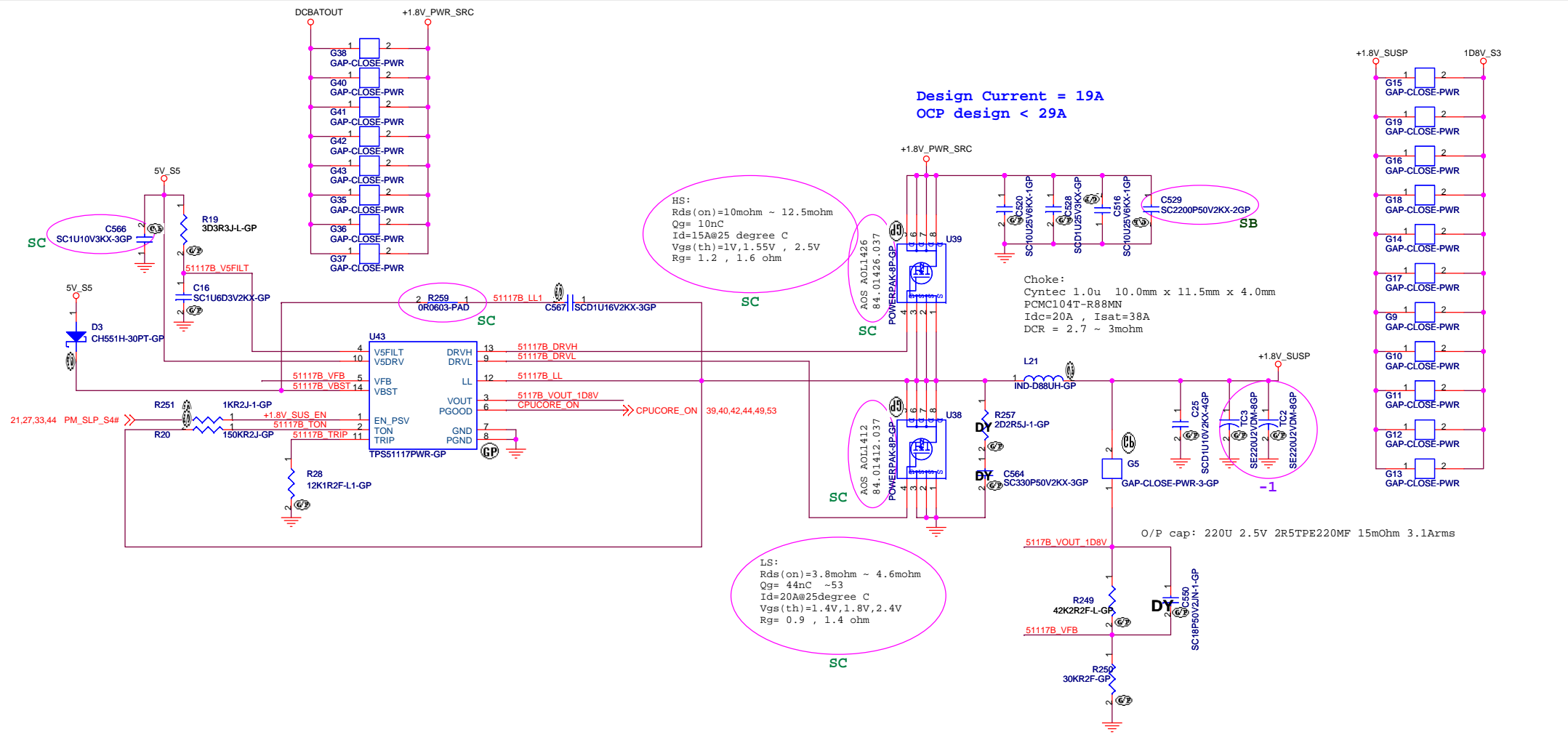
Title			DC-DC VCCCPUCORE 2/2
Size	Document Number	Rev	
A3	Hawke-Intel	-2	
Date:	Thursday, November 22, 2007	Sheet	41 of 58

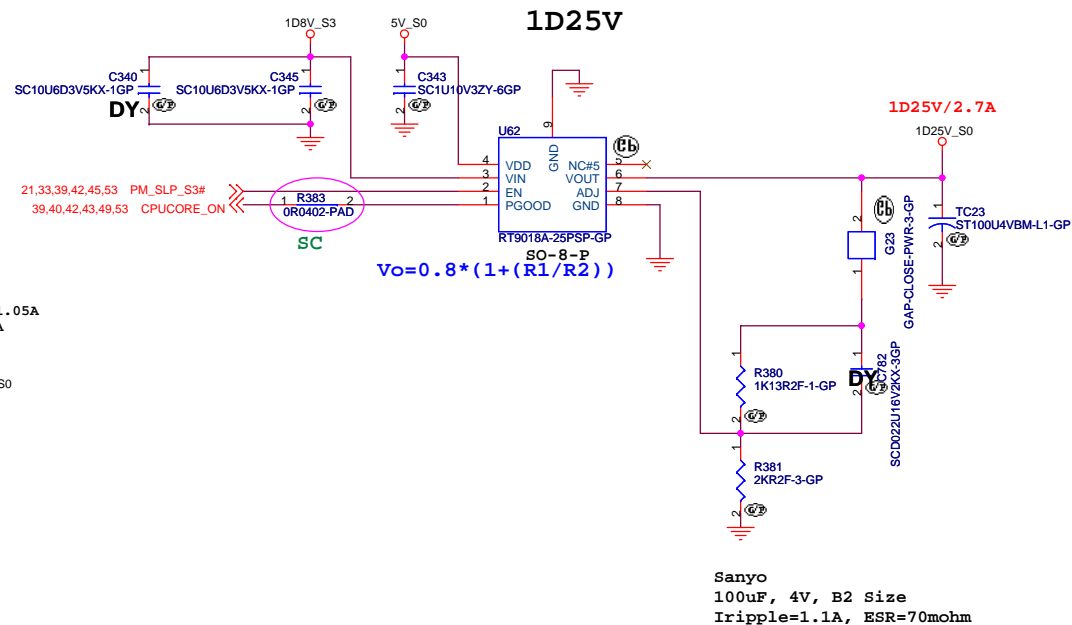
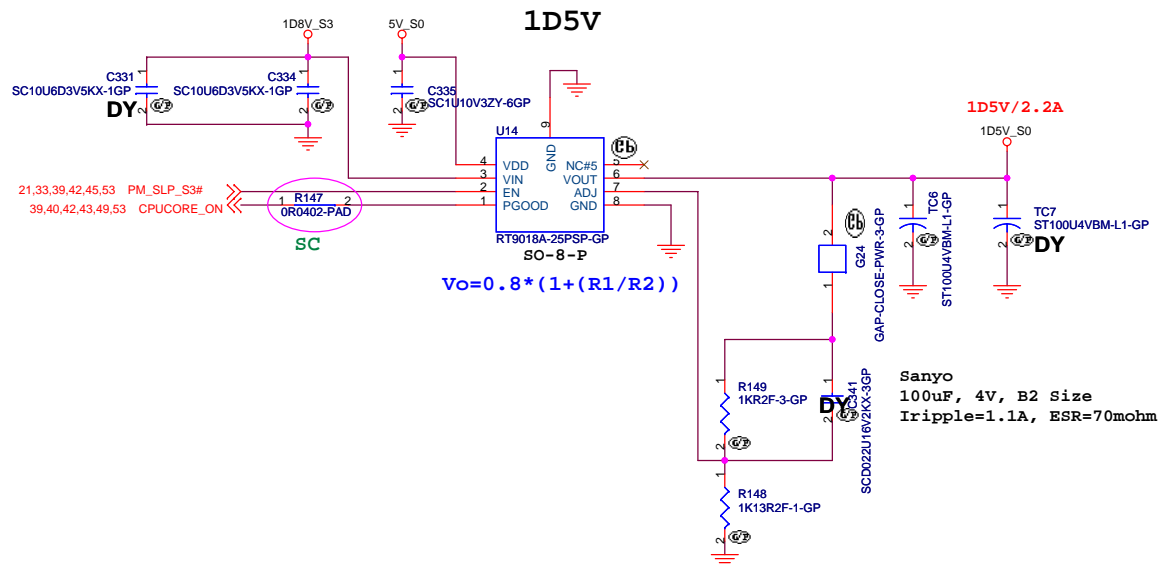


<Core Design>

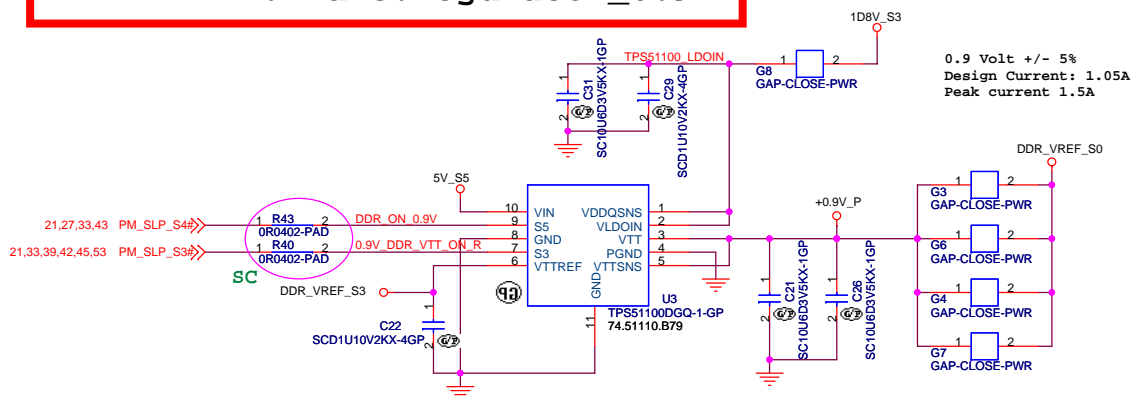
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			DCDC 1.05V	
Size	Document Number	Rev		
A3	Hawke-Intel	-2		
Date:	Thursday, November 22, 2007	Sheet	42	of 58





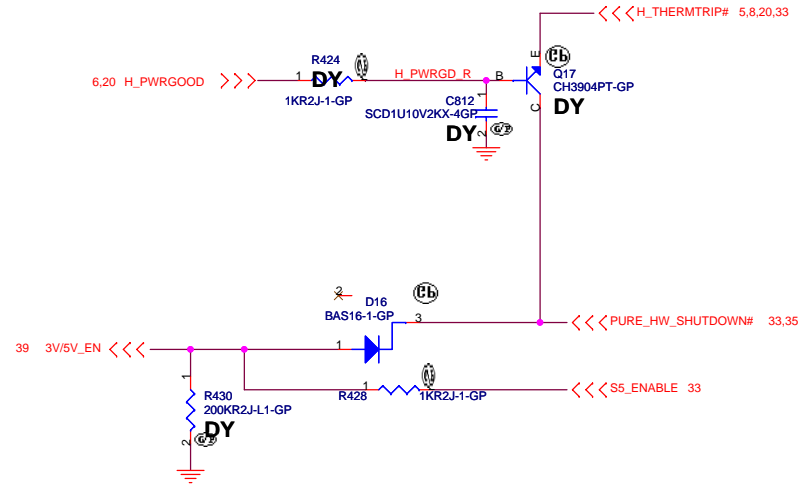
SSID = PWR.Plane.Regulator_0.9V



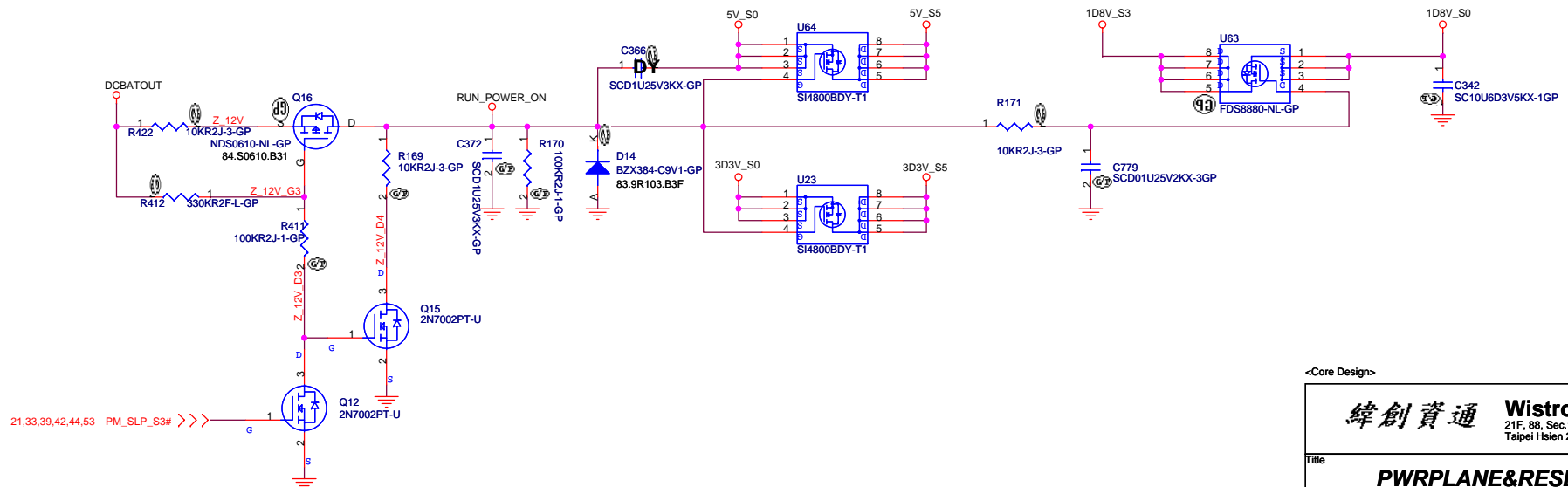
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DC to DC 1D5V / 0D9V / 1D25V		
Size	Document Number	Rev
A3	Hawke-Intel	-2
Date:	Thursday, November 22, 2007	Sheet 44 of 58



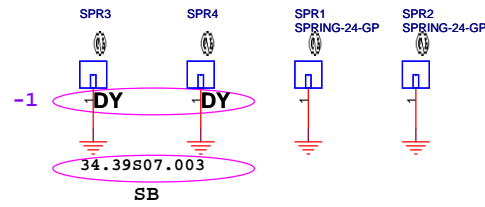
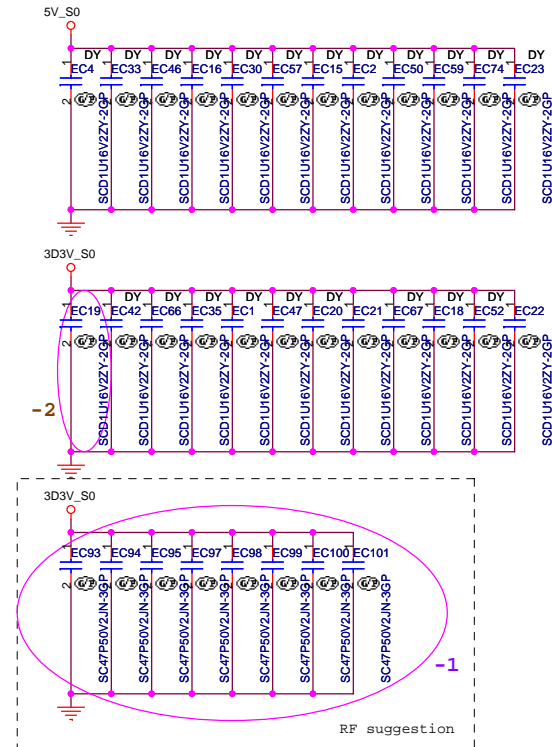
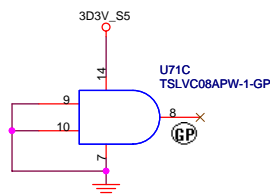
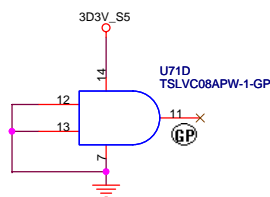
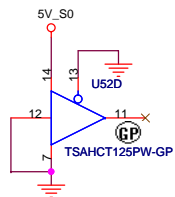
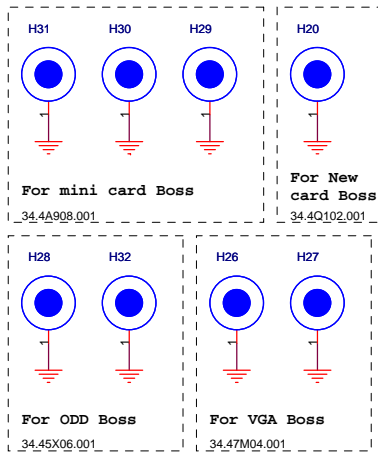
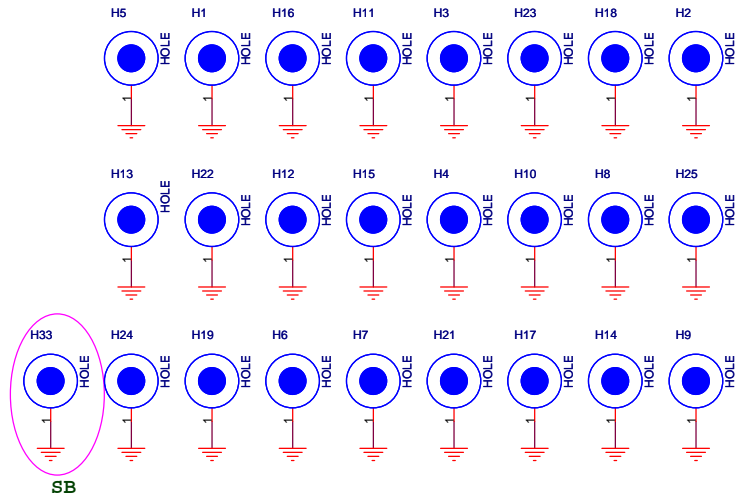
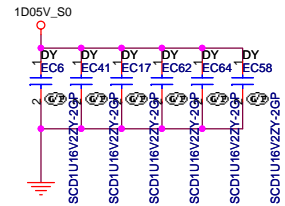
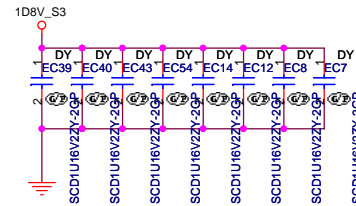
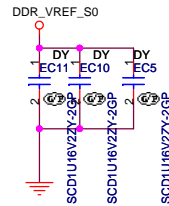
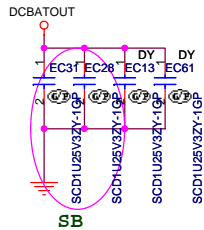
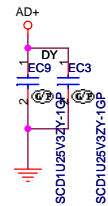
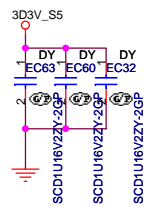
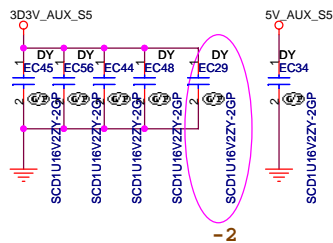
Run Power

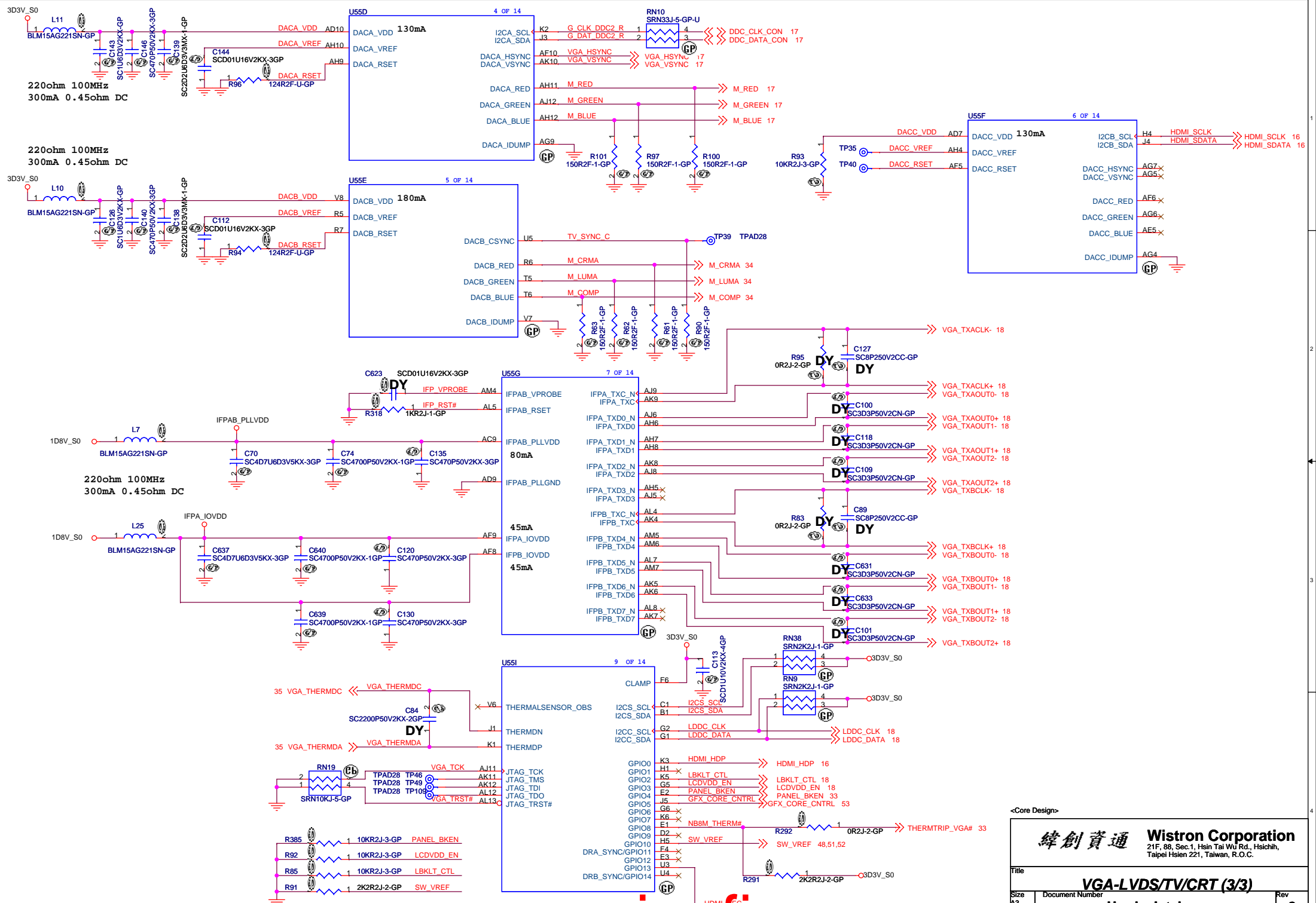


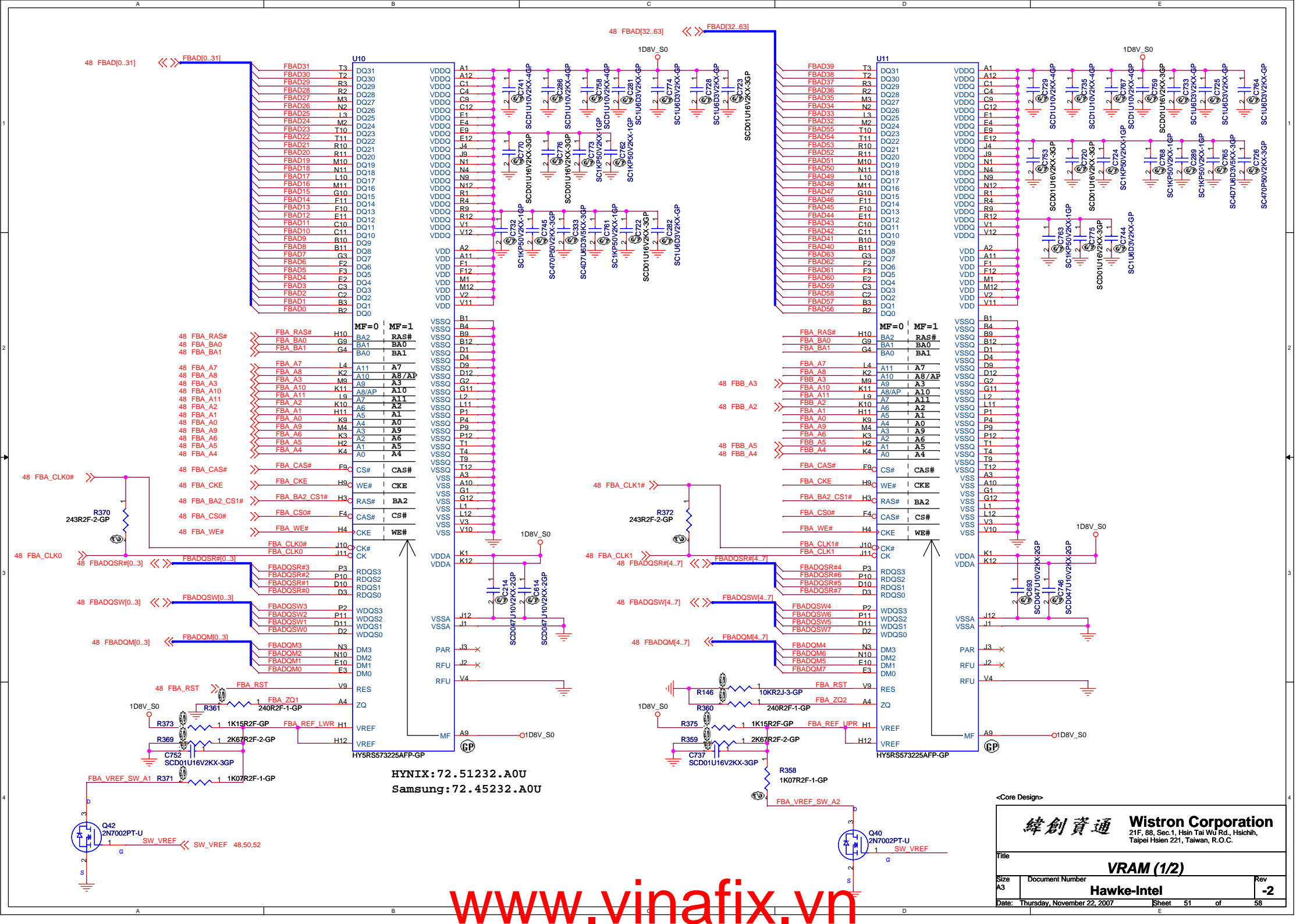
<Core Design>

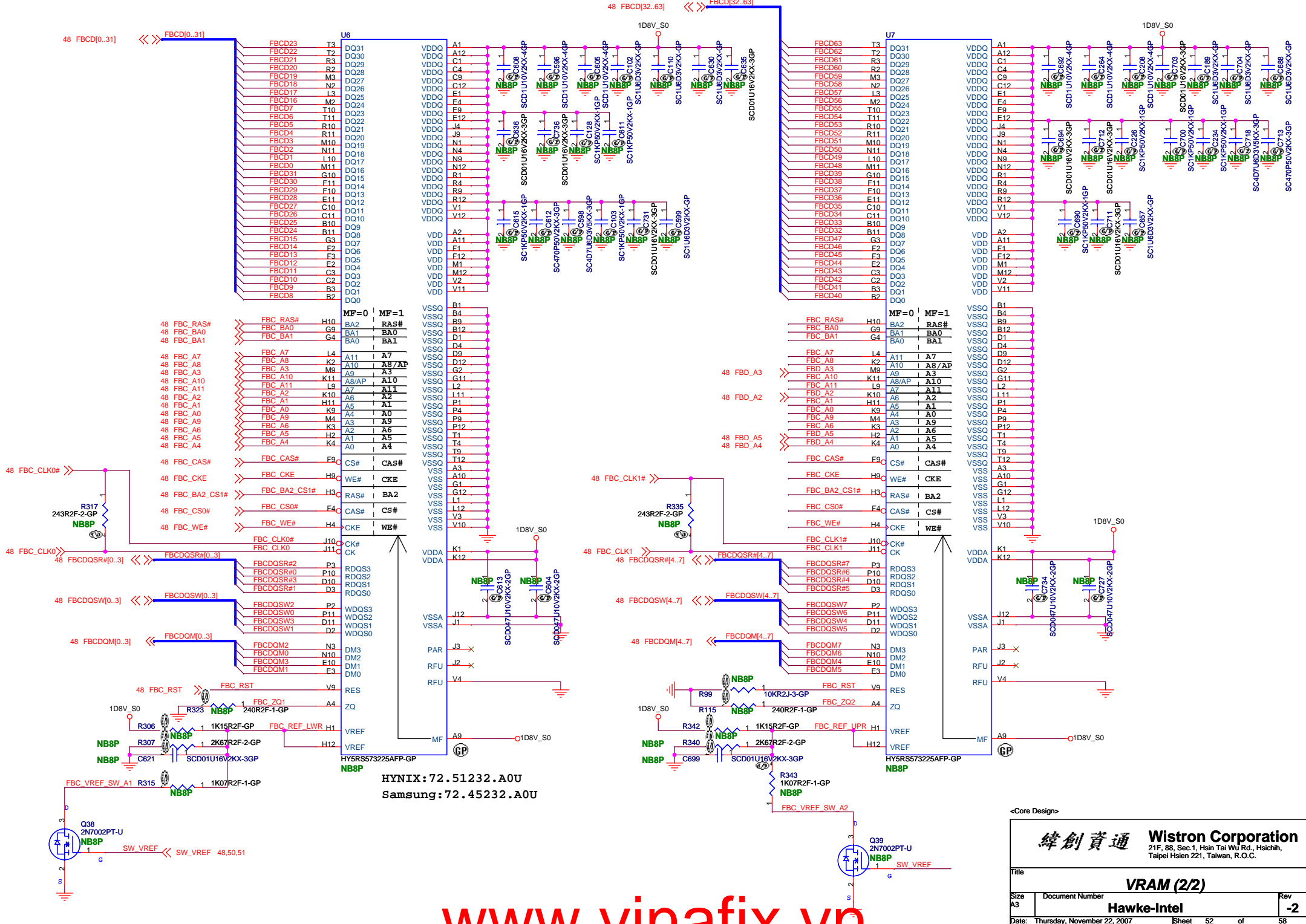
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

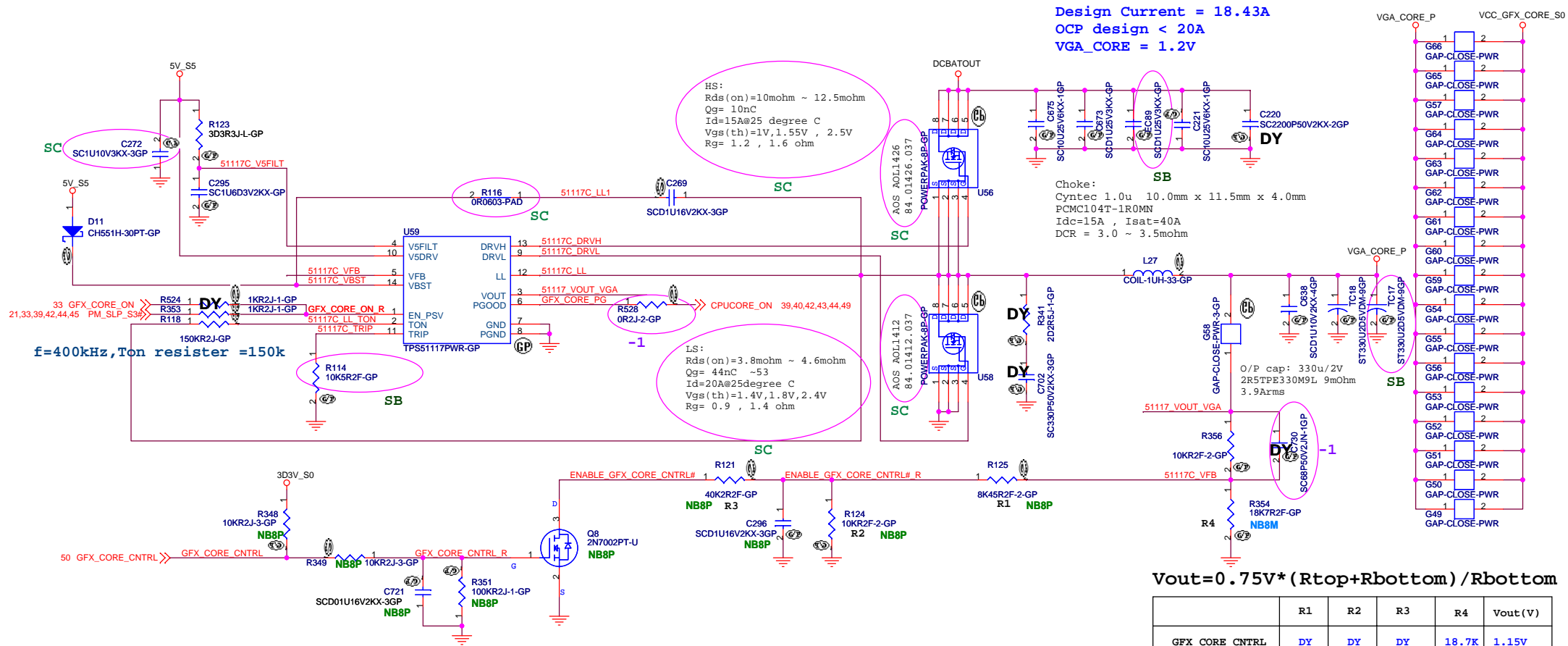
Title		PWRPLANE&RESETLOGIC	
Size A3	Document Number	Hawke-Intel	Rev -2
Date: Thursday, November 22, 2007	Sheet 45	of 58	



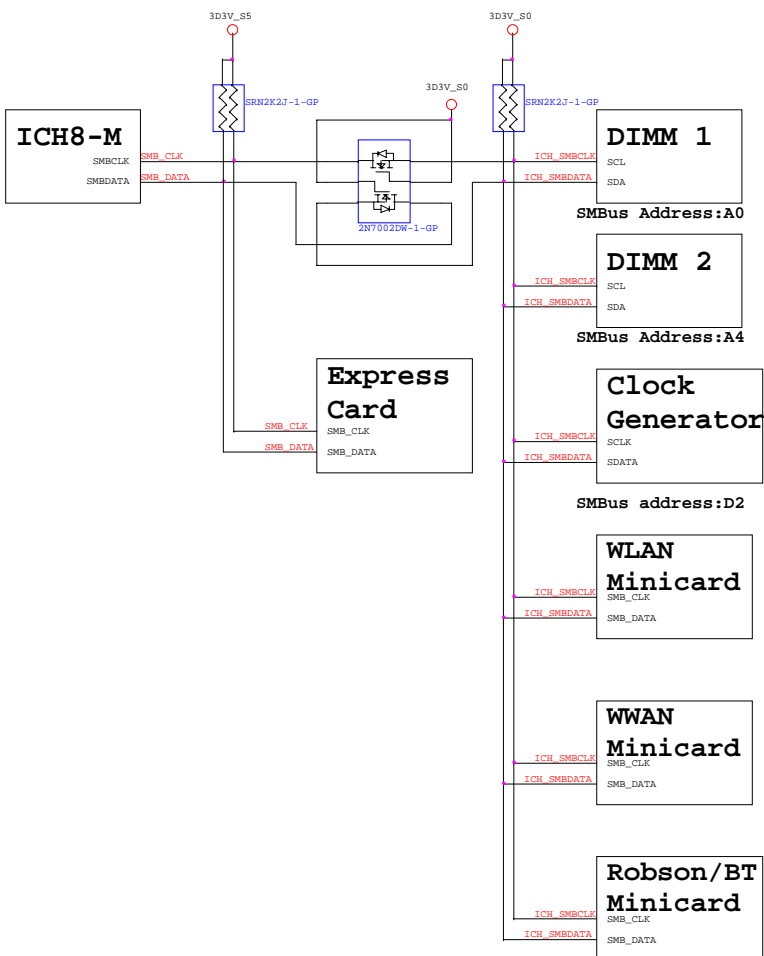




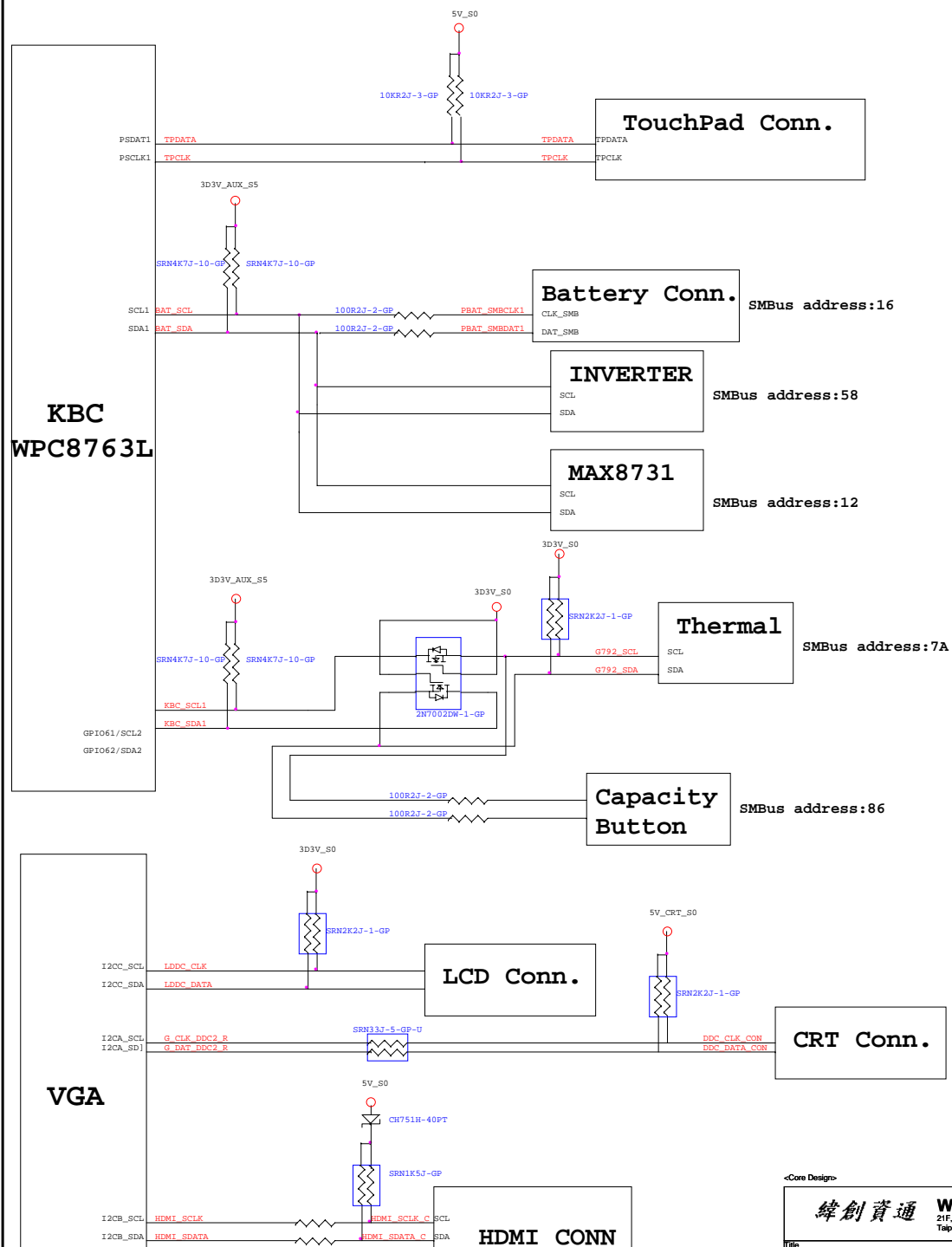




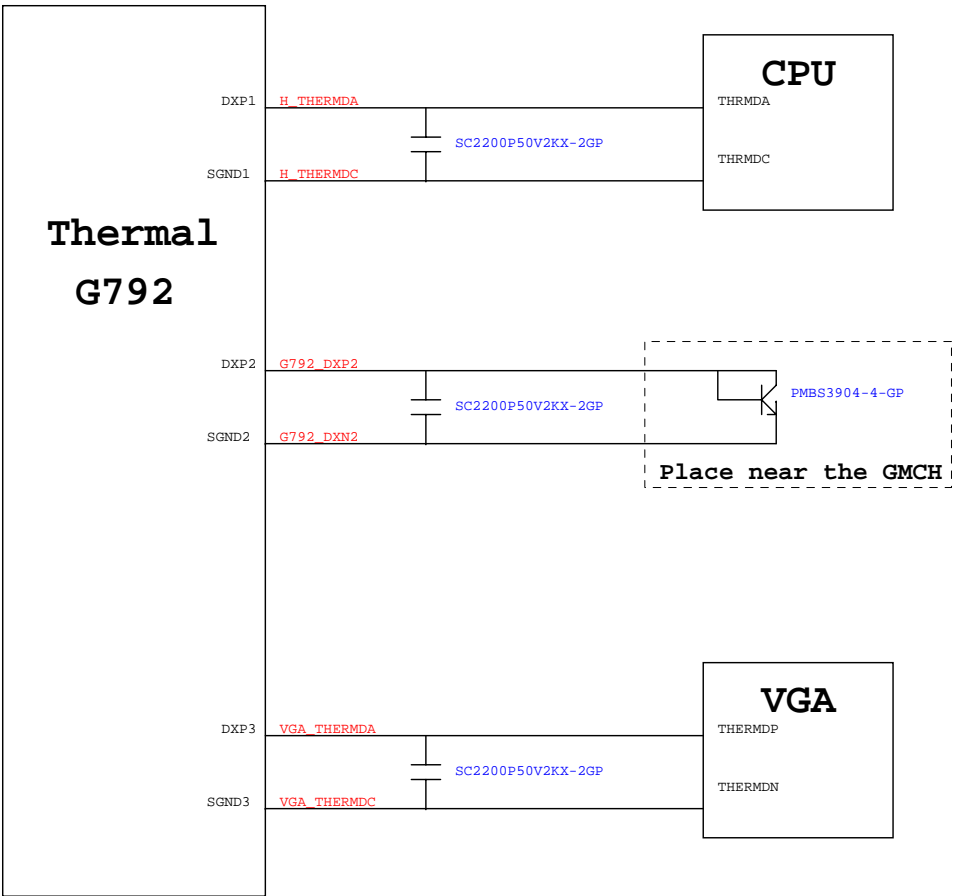
ICH8 SMBus Block Diagram



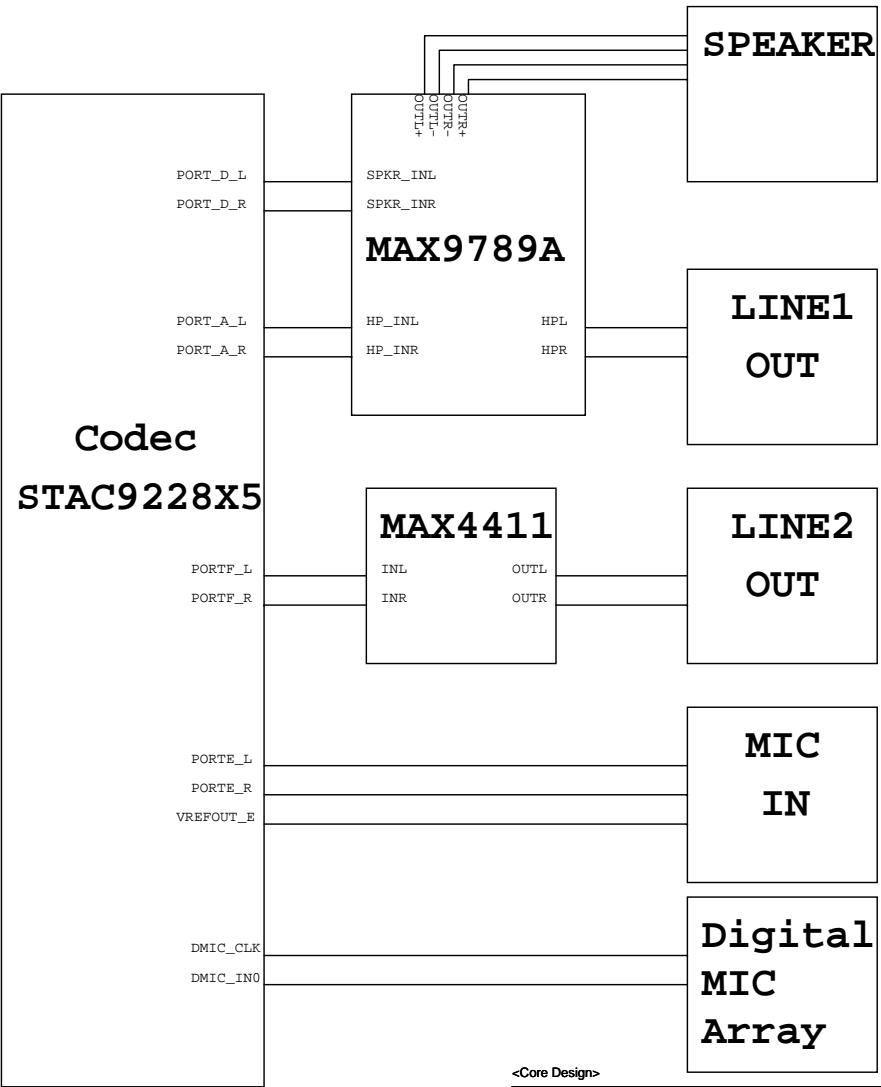
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/06	X00 to X01	1	4	Changed R431 from 10K ohm to 2.2K ohm.	Follow M08 design.	EE
		2	4	Changed X4's CL from 20pF to 10pF and changed C392 and C399 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		3	4	Changed RN27, RN28, RN29 and RN31 from 0 ohm to 22 ohm.	To solved these clock signals' Slew Rate are over spec.	EE
		4	18	Changed LVDS connector from 42-pin to 40-pin.	By ME suggestion.	ME
		5	18,33	Connected the LCD1 pin 3 to GND and connected pin 6 to WPC8763's GPIO05 (pin 108 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the LCD cable PAID.	EE
		6	18	Added EC75-EC78 near CAMERA1.	By EMC team suggestion.	EMC
		7	20	Change C354 and C355 from 15pF to 12pF and changed X1 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		8	21	Added R526 10K ohm between GPIO26 and 3D3V_S0, removed R404.	To solved 3D3V_S0 has leakage when S3 and S5.	EE
		9	21	Added the reserved Q47, D31, R530, R531 and R532.	For test EC_RMRST#_R circuit.	EE
		10	21	Changed R442 from 22.6 ohm to 20 ohm.	To sloved the left side USB ports and Camera USB's eye diagram fail.	EE
		11	23	Changed HDD connector.	By ME suggestion.	ME
		12	25	Changed 1394 connector.	To used reverse type by ME suggestion.	ME
		13	25	Changed X5's CL from 20pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		14	25	Removed R466, U26, R192 and D19, and connected the net MC_PWR_CTRL_0 to U25 pin 4.	For these materials are no used.	EE
		15	25	Populated C887, C888 and C894-C896.	By EMC team suggestion.	EMC
		16	26	Changed C387 and C390 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		17	27	Changed RJ1 connector.	By ME suggestion.	ME
		18	30	Changed U61 from 8Mbits to 16Mbits SPI ROM.	By customer requirement.	EE
		19	30	Added EC79-EC82 near CAP1.	By EMC team suggestion.	EMC
		20	30	Added EC83-EC88 near BT1.	By EMC team suggestion.	EMC
		21	30	Added EC90-EC91 near CN2 (Biometric).	By EMC team suggestion.	EMC
		22	31	Changed C880 and C881 from 0402 size to 0603 size.	Follow Thurman design.	EE
		23	32	Swaped the nets AUD_HP1_OUT_R1, AUD_HP1_OUT_L1 with AUD_AMP_GAIN1, AUD_AMP_GAIN2.	To sloved the HP1 hadn't output.	EE
		24	32	Changed R211 and R212 from 100K ohm to 10M ohm.	To sloved the AUD_HP1_EN and AUD_HP2_EN volatge level lower than 2V.	EE
		25	33	De-pop R396 and populated R395.	To changed the MB version id to SB.	EE
		26	33	Changed R391 and R405 from 10K ohm to 100K ohm.	To sloved the INSTANT_BTN# and SNIFFER_PWR_SW# can't work.	EE
		27	33	Added R527 100K ohm between WLAN/BT_BTN# and 3D3V_AUX_S5.	To sloved the WLAN/BT_BTN# can't work.	EE
		28	33	Changed X2 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		29	33,36	Changed KB1 from 25-pin to 27-pin connector, connected the KB1 pin 27 to GND and connected pin 26 to WPC8763's GPI92 (pin 99 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the KB cable PAID.	ME,EE
		30	33	Changed R408 and R389 from 10K ohm to 4.7K ohm.	By Vendor's FAE suggestion.	EE
		31	35	Changed FAN1 from 4-pin to 3-pin connector.	By ME suggestion.	ME
		32	36	Added R534, Q48 and R535 off SATA_LED# and Q23.	Supported the HDD LED is dim when sinffer switch press.	EE
		33	36	Connected LED2 pin A from 5V_S0 to 5V_S5.	To sloved the Power LED can't breath when system enter S3.	EE
		34	38	Changed C530 and C531 from 1206 size to 1210 size and populated C7.	To solved noise when battery full load.	Power
		35	39	Changed R477 from 12.1K ohm to 13.3K ohm and changed R468 from 12.1K ohm to 11.8K ohm.	To adjust 3.3V and 5V current limit by power team suggestion.	Power
		36	40	Changed R7 from 12.7K ohm to 11.8K ohm and changed R468 from 3.24K ohm to 3.65K ohm.	To adjust CPU Vcore current limit by power team suggestion.	Power
		37	42	Changed R135 from 12.1K ohm to 11K ohm .	To adjust 1.05V current limit by power team suggestion.	Power
		38	43	Populated C529.	By EMC team suggestion.	EMC
		39	46	Added more one hole H33.	By EMC team suggestion.	EMC
		40	46	Populated EC28 and EC31.	By EMC team suggestion.	EMC
		41	47	Added C900, C901, C904 10uF and TC26 100uF.	To sloved VGA Vcore had OVP when run 3Dmark.	Power
		42	53	Changed R135 from 12.1K ohm to 10.5K ohm .	To adjust CPU Vcore current limit by power team suggestion.	Power
		43	53	Added EC89 0.1uF between DCBATOUT and GND.	By EMC team suggestion.	EMC

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY from X00 to X01

Size
A3

Document Number

Hawke-Intel

Rev

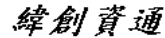
-2

Date: Thursday, November 22, 2007

Sheet 56 of 58

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/08/17	X01 to X02	1	4	Changed U22 from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	Changed clock gen symbol from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	EE
		2	15	Changed HDMI power rail from +5V_HDMI to 5V_S0.	Follow Thurman design.	EE
		3	17	Populated D4, D5, D6, D7 and D8.	By NV GPU ESD requirement.	EMC
		4	17	Changed L1, L2 and L4 from BLM18BA100SN1 to BLM18BB470SN1	To solve the ring on RGB singnal.	EE
		5	18,33	Added D32, connected pin 1 to LCDVDD_TST_EN, pin 2 to LCDVDD_EN and pin 3 to ENVDD. Changed R276 from 0 to 100k ohm and changed R276.1 to GND	Added LCDVDD_TST_EN from U17.27 to control U53.3	EE
		6	18	Disconnted LCD1 pin 3 and pin 10	To prevent the power short to GND.	EE
		7	21	Added R542 for ECSCI# need to pull up 3D3V_S0	To solve one of CPU core always loading 100%.	EE
		8	27	Added EC92 22pF between NEWCARD_CLKREQ# and GND	By EMC team suggestion.	EE
		9	27	Added note for transformer source part number.	By EMC team suggestion.	EE
		10	29	1.Changed D20 to U73 for Bluetooth Action circuit. 2.Reserved U73, R193 and R195, populated R194.	1.It can be used both BT module and BT mini-card. 2.Just keep BT module now.	EE
		11	29, 33	Connect MINI2 pin 20 to U17.24 (GPO47 of KBC).	Changed WWAN enable WiFi RF controlled by another GPIO pin (U17.24 is GPO47 of KBC).	EE
		12	30, 33	Rename SNIFFER_YELLOW# to SNIFFER_YELLOW, SNIFFER_BLUE# to SNIFFER_BLUE.	These pins are High active.	EE
		13	30	Disconnted SNIFFER_BD1 pin 8 and CAP1 pin 7.	To prevent power short to GND.	EE
		14	30	Changed EC90 and EC91 from 22pF to MLVG0402220NV05BP.	By EMC team suggestion.	EMC
		15	32	Populated EC24, EC25, EC26 and EC27 and change to 1000pF.	By EMC team suggestion.	EMC
		16	32	Changed Q45 to U47 and added R543.	To add AUD_SPK_ENABLE# controlled by AMP_MUTE#.	EE
		17	32	Changed R197 from 0 ohm to 100K ohm and pull up to +5V_SPK_AMP, dispopulated R505 and populated R213.	To solve HP1, HP2 and Speaker have "BoBo" noisy when power on, off, enter S3.	EE
		18	33	Populated R396 and R398, dispopulated R395 and R399.	Change Board ID to version SC.	EE
		19	36	Populated Q48 and R534, dispopulated R535.	HDD LED should be dim when power on by Sniffer button.	EE
		20	36	Changed C275 and C276 from reserved 33pF to MLVG0402220NV05BP, and populated them	By EMC team suggestion.	EMC
		21	36	Changed KB EMI caps from 220pF to 180pF.	To solved the word has repeat symptom when key-in.	EE
		22	38	The U42 and U44 were swap the main source and 2nd source.	To prevented used AO4468 that SI4800BDY 2nd source on charger H/S and L/S MOS.	EE
		23	39	Populated R485 and dispopulated R489.	To changed 3V and 5V PWM to Skip mode.	EE
		24	42, 43, 53	Changed C329, C566 and C272 rated voltage from 6.3V to 10V.	For derating issues by power team requirment.	EE
		25	43, 53	Change the U56 and U39 from 2nd source to main source, and swap the U38 and U58's the main source and 2nd source	To combined U39 and U56 material item of BOM with CPU H/S MOS (U4 and U35).	EE
		26	20	Changed C354 and C355 from 12pF to 8.2pF.	For Negative Resistance of X1 isn't enough.	EE
		27	33	Changed C350 and C351 from 15pF to 10pF.	For Negative Resistance of X2 isn't enough.	EE

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
HISTORY from X01 to X02	
Size A3	Document Number
	Hawke-Intel
Date: Thursday, November 22, 2007	Sheet 57 of 58
	Rev -2

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/09/07	X02 to A00	1	4	Changed U22 from Realtek RTM875M-606-LF to ICS 9LPRS365BKLFT.	Changed clock gen symbol from Realtek RTM875M-606-LF to ICS 9LPRS365BKLFT.	EE
		2	23	1.Added Q49, Q50, U75, U76, R544, R545, R547, R548, R549, R551, C907, C908 and reserved R546, R550. 2.Change HDD1 VDD from 5V_S0 to 5V_HDD, CDROM1 VDD from 5V_S0 to 5V_MOD. 3.Added HDDC_EN on GPIO27 (U17 pin11)	Added HDD and ODD power controlled circuit.	EE
		3	25	Changed SKT1394 to SUYIN 020115FR004S536ZR.	The original is hard to pull out the 1394 cable.	ME
		4	29	Reserved R552 and R553 on U73 input pin.	Reserved for U73 populated.	EE
		5	29	Added EC102 and EC103.	To solve SIM card data has crosstalk with clock.	EE
		6	31, 32	Changed the R501, R503, L42, L43, L40 and L41 from 0 ohm to BLM18DB601SN1D, and changed EC68-EC73 to 220pF.	To solve the audio can't pass HP1 THD+N noise.	EE
		7	33	Changed the WWAN_EN from GPO47 (U17 pin24) to GPIO26 (U17 pin10).	For GPO47 is strap pin of KBC and it can't pull down.	EE
		8	33	Populated R395, and dispopulated R396.	Changed Board ID to -1	EE
		9	34, 37	Populated U45 and U51, and dispopulated F2 and F3.	Changed USB power controll by power switch.	EE
		10	36	Changed KB EMI caps from 180pF to 220pF.	Back to X01 BOM.	EE
		11	46	Added EC93-EC95 and EC97-EC101.	Added 8pcs 0.1uF near GPU by RF team suggestion.	RF
		12	53	Dispopulated C730.	To solved the system would be shut down when VRAM over clock to 850MHz.	EE
		13	36	Changed KB connector from 27-pin to 25-pin.	The KB connector of 27-pin has quality issue. No support KB PAID.	EE
		14	4	Changed RN35 from 0 ohm to 33 ohm.	The 27MHz has under shoot over spec.	EE
		15	20	Changed C354 and C355 from 8.2pF to 5.6pF.	To solved RTC can't meet criterion.	EE
		16	37	Depop D1, D2, D21 and D22.	To solved battery leakage can't meet criterion.	EE

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/11/15	A00 to A01	1	27	1. Changed R433 from 0 ohm to 20 ohm, and populated C819. 2. Added C909 10pF closed MINI3. 3. Added C911 15pF closed MINI2. 4. Added C910 10pF closed MINI1.	To improve the PLT_RST1# has shoulder.	EE
		2	24	Added R554, and dispopulated EC102 and EC103.	To solve SIM card data has crosstalk with clock.	EE
		3	33	Populated R399, and dispopulated R398.	Changed Board ID to -2	EE
		4	41	Added TC27 and removed C538.	To decrease CPU cap singing noise.	EE
		5	37, 46	Change pin 2 of D1, D2, D21 and D22, pin 1 of EC29 from 3D3V_S5 to 3D3V_AUX_S5.	To saved battery life under S4 and S5.	EE